

Compal Confidential

QLA13/15 LA8502P Schematics Document

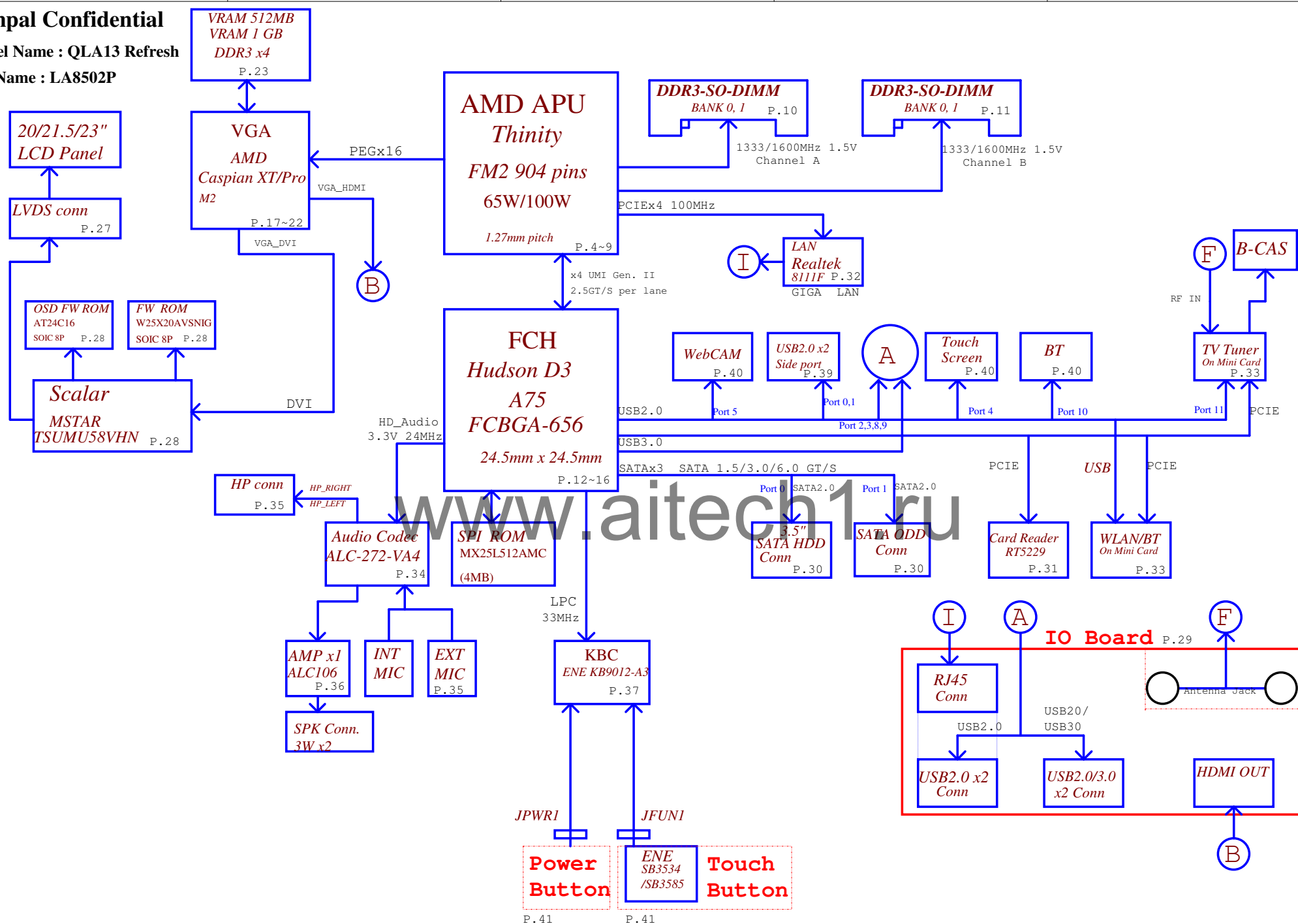
AMD Trinity APU/NPU with DDRIII + FCH Hudson D3
www.aitech1.ru
AIO M/B

Thursday, January 24, 2013

REV:1.0

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File Name : LA8502P



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Issued Date	2011/09/12	Deciphered Date	2012/09/12	Title	Block Diagrams		
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Voltage Rails

Power Plane	Description	S1	S3	S5
+12V1	Adapter power supply (12V)(For V_5V;V_3.3V;1.5V;12VS)	ON	ON	OFF
+12V2	Adapter power supply (12V)(For VGA_CORE;1.05VS;VRAM_1.5VS;CPU_CORE;VGFX_COREP)	ON	ON	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Graphics voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail once PS_ON# low	ON	ON	OFF
+3VSB	3.3V power rail befor PS_ON# low	ON	ON	ON
+3.3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+V_3.3V	3.3V power rail once Adapter plug-in	ON	ON	OFF
+V_5V	5V power rail once Adapter plug-in	ON	ON	OFF
+5VSB	5V power rail befor PS_ON# low	ON	ON	ON
+5VALW	5V always on power rail once PS_ON# low	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+3VS_DGPU	3.3V power rail for GPU	ON	OFF	OFF
+VGA_CORE	Graphics power rail for GPU	ON	OFF	OFF
+1.05VS_DGPU	1.05VS switched power rail for GPU	ON	OFF	OFF
+VRAM_1.5VS	1.5VS power rail for VRAM	ON	OFF	OFF

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
ALC106	0100_100xb	48H	EMC1412-A (dGPU)	1111_100xb	F8H
			SB-TSI	1001-100xb	98H
			CPU CORE(IR3565MCP02TRP)		0x08

PCH SM Bus address

Device	Address	
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
DDR DIMM3 (FCH_SMB0)	1001-010xb	94
DDR DIMM4 (FCH_SMB0)	1001-011xb	96

	Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2	
X7648938L01	HYN 1G-1@	L	L	L	VRAM_ID0L@ VRAM_ID1L@ HYN 1G-1@
X7648938L02	SAM1G- 1@	H	L	L	VRAM_ID0H@ VRAM_ID1L@ SAM1G-1@
X7648938L03	HYN1G-2@	L	H	L	VRAM_ID0L@ VRAM_ID1H@ HYN1G-2@
X7648938L04	SAM1G-2@	H	H	L	VRAM_ID0H@ VRAM_ID1H@ SAM1G-2@

R1	SA00003YO00	HYN 1G-1@	S IC D3 128MX16 H5TQ2G63BFR-11C FBGA 96P
R3	SA00003YO40		S IC D3 128M16 H5TQ2G63BFR-11C 96P C38A!
R1	SA000047Q00	SAM1G-1@	S IC D3 128M16 K4W2G1646C-HC11 FBGA 96P
R3	SA000047Q30		S IC D3 128M16 K4W2G1646C-HC11 96P C38A!
R1	SA00003YOA0	HYN1G-2@	S IC D3 128MX16 H5TQ2G63DFR-11C FBGA C38
R3	SA00003YOD0		S IC D3 128MX16 H5TQ2G63DFR-11C C38A!
R1	SA00005SH00	SAM1G-2@	S IC D3 128MX16 K4W2G1646E-BC11 FBGA 96P
R3	SA00005SH20		S IC D3 128MX16 K4W2G1646E-BC11 C38A!

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VSB	+VS
Full ON		HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)		LOW	LOW	LOW	OFF	ON	OFF

BTO Option Table

BTO Item	BOM Structure
MBSC@	VGA@
HWTV@	UMA@
USB3@	DIS@
DIS@	W/ DIS
Hynix VRAM (512M)	HYN512@
Samsung VRAM (512M)	SAM512@
Hynix VRAM (1G)	HYN1G@
Samsung VRAM (1G)	SAM1G@

SKU ID(Project) Table

Project_ID2 (GPIO191)	Project_ID1 (GPIO190)	Project_ID0 (GPIO189)	SKU	BOM CONTROL @
0	0	0	X	
0	0	1	X	
0	1	0	X	
0	1	1	X	
1	0	0	X	
1	0	1	X	
1	1	0	DIS_512M_NPU	GPIO189L@ GPIO190H@ GPIO191H@ DIS@ MB@ X7636838L04
1	1	1	DIS_1G_NPU	GPIO189H@ GPIO190H@ GPIO191H@ DIS@ MB@ X7648938L01

	Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2		VRAM_ID0L@	R1233	SD028100280
X7636838L04	Hynix 512	L	L	L	VRAM_ID0L@ VRAM_ID1L@ HYN512@	VRAM_ID1L@	R1234	SD028100280
X7636838L03	Samsung 512	L	H	L	VRAM_ID0L@ VRAM_ID1H@ SAM512@	VRAM_ID0H@	R1230	SD028100280
						VRAM_ID1H@	R1231	SD028100280

R1	SA000041S20	HYN512@	S IC D3 64MX16 H5TQ1G63DFR-11C FBGA 96P
R3	SA000041S70		S IC D3 64M16 H5TQ1G63DFR-11C FBGA C38A!
R1	SA00004GS00	SAM512@	S IC D3 64M16 K4W1G1646G-BC11 FBGA 96P
R3	SA00004GS50		S IC D3 64M16 K4W1G1646G-BC11 FBGA C38A!

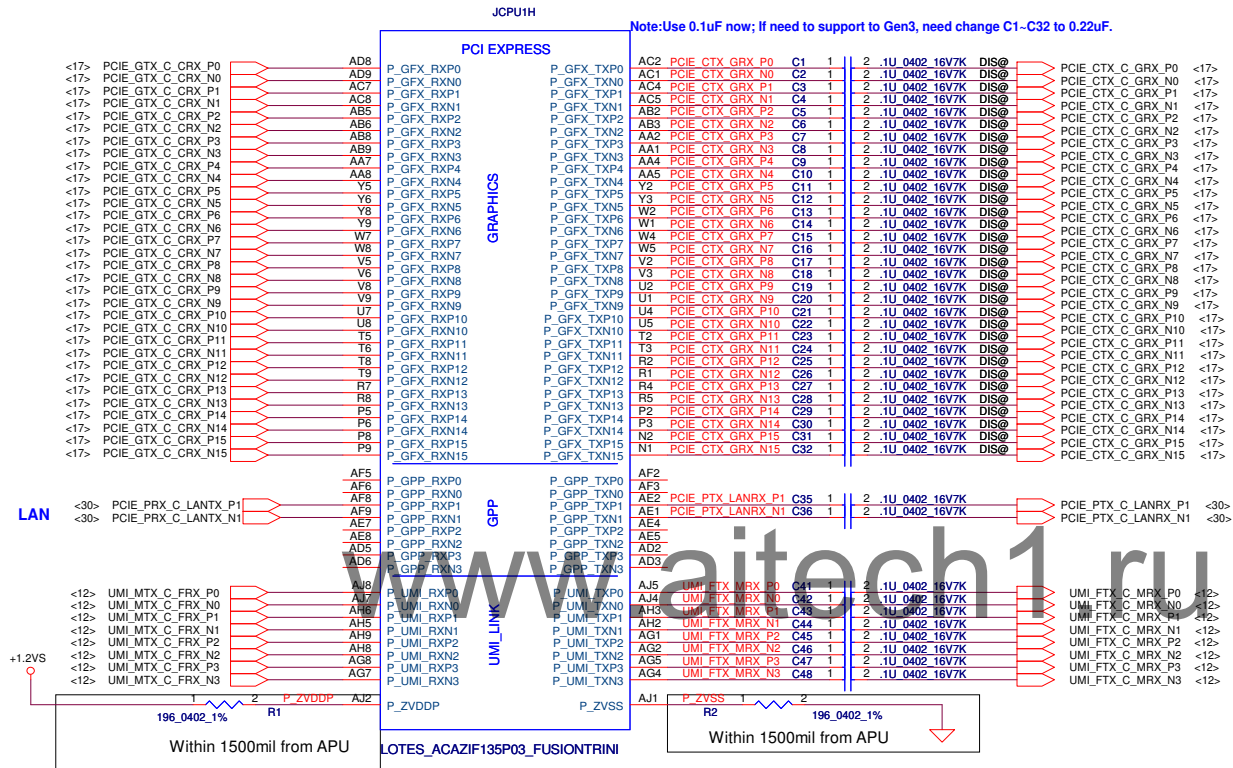
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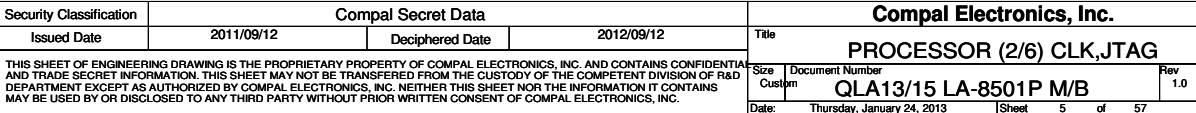
BOARD ID Table

Board ID	Ra/Rb	Vad-bid
NON AV SKU	R445 0 ohm	0 V

USB Port Table

USB 2.0	USB 1.1	Port	Device (D3 Only)
	OHCI	0	NC
		1	NC
EHC11 DEV18 Fn2	OHCI	0	USB Conn B
		1	USB Conn B
		2	Touch Screen
		3	Camera
EHC12 DEV19 FN2	OHCI	4	USB Conn R
		5	MINI(WALN+BT)
		6	BT
		7	Mini Card(TV Tuner)
EHC13 DEV22 Fn2	OHCI	8	HWTV
		9	USB Conn R
		10	
		11	
xHCI DEV16 Fn0 (D3 Only)	xHCI	12	USB30 Conn3
		13	USB30 Conn4
		0	
xHCI DEV16 Fn1	xHCI	1	
		2	USB 3.0 Port2
		3	USB 3.0 Port3

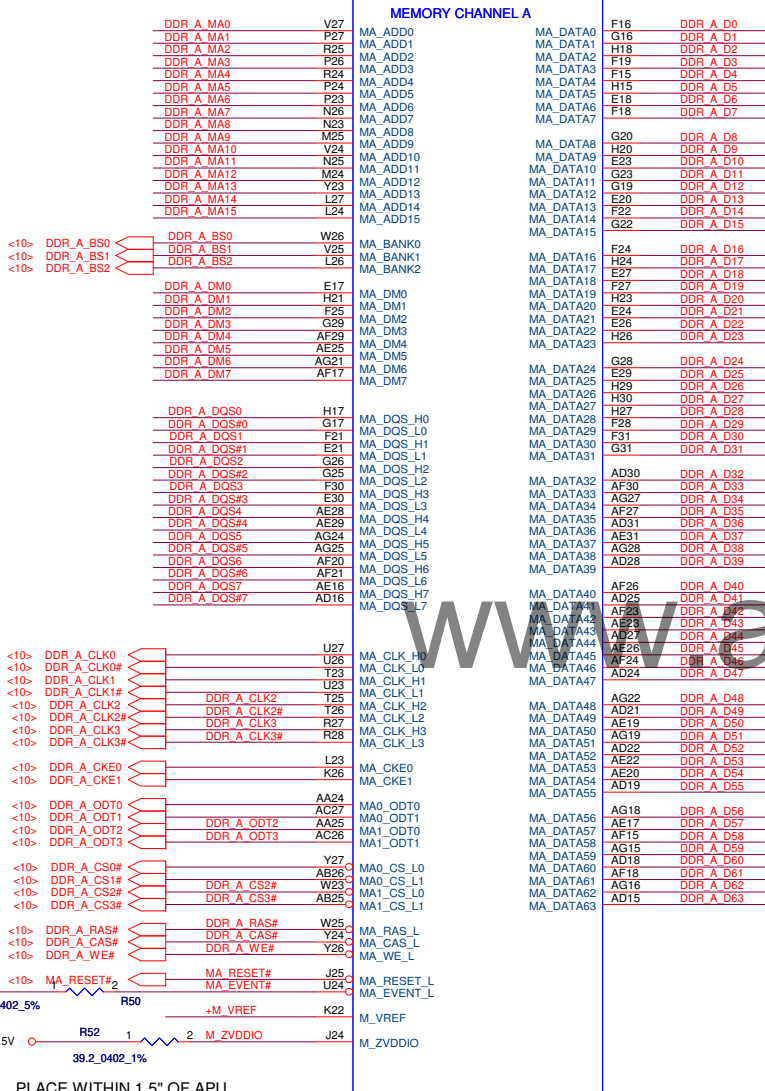




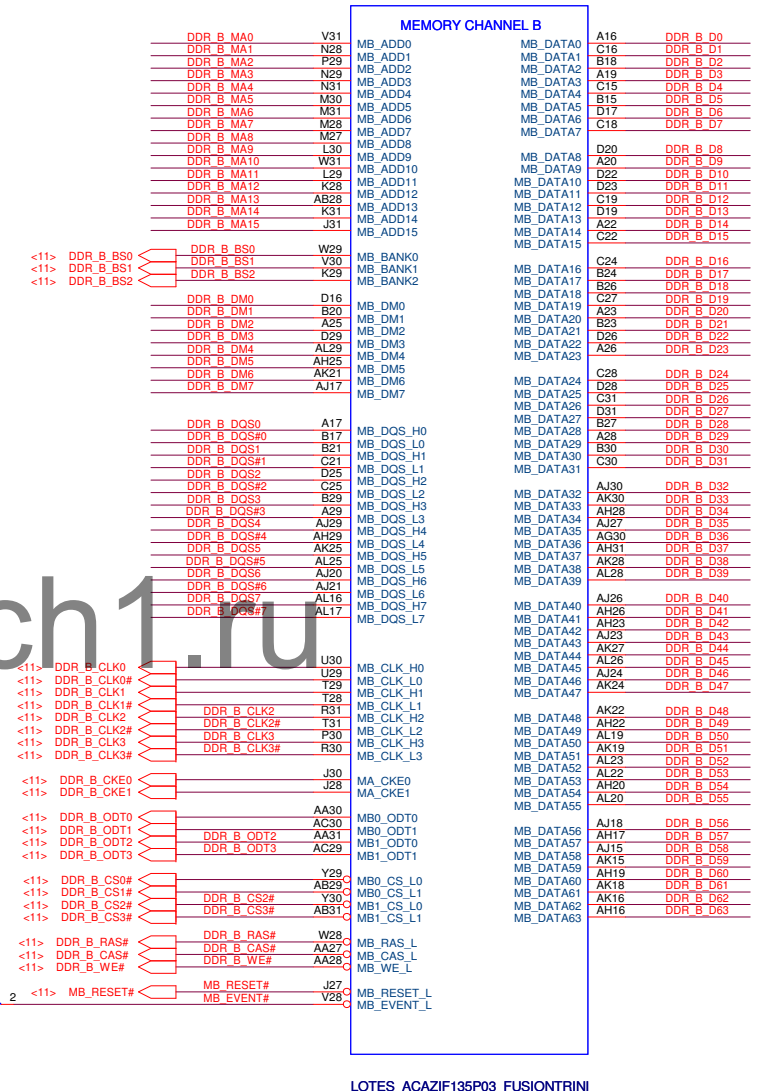


JCPU1A

JCPU1B



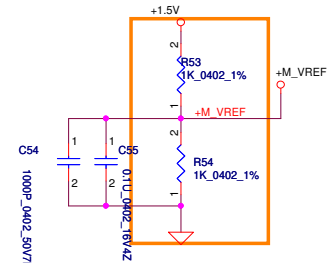
LOTES_ACAZIF135P03_FUSIONTRINI



LOTES_ACAZIF135P03_FUSIONTRINI

1116 modify

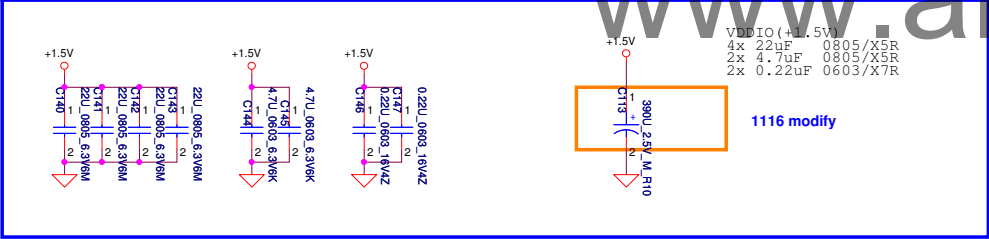
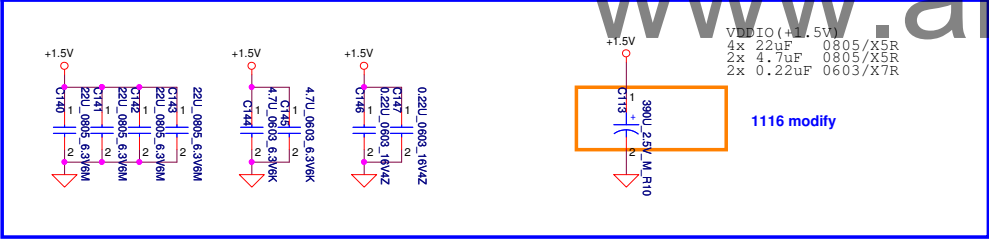
PLACE WITHIN 1.5" OF APU



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+CPU_CORE At PWR Page53

+CPU_CORE_NB At PWR Page53



VDDP_A
C1694, C1695, C1696, C1697

VDDP_B
C1708, C1709, C1710

VDDR
C1715, C1716, C1717, C1718, C1719

FM1
Top View

1x 10uF
4x 4.7uF
2x 0.22uF
2x 180pF
0805/X5R
0805/X5R
0603/X7R

+1.5V
C86 100u 0603, 6.3V6M
1 2

+1.5V
C91 4.7u 0603, 6.3V6K
C92 4.7u 0603, 6.3V6K
C93 4.7u 0603, 6.3V6K
C94 4.7u 0603, 6.3V6K
1 2

+1.5V
C95 0.22u 0603, 16V4Z
C97 0.22u 0603, 16V4Z
C98 0.22u 0603, 16V4Z
1 2

+1.5V
C97 180p 0402, 50V3J
C98 180p 0402, 50V3J
1 2

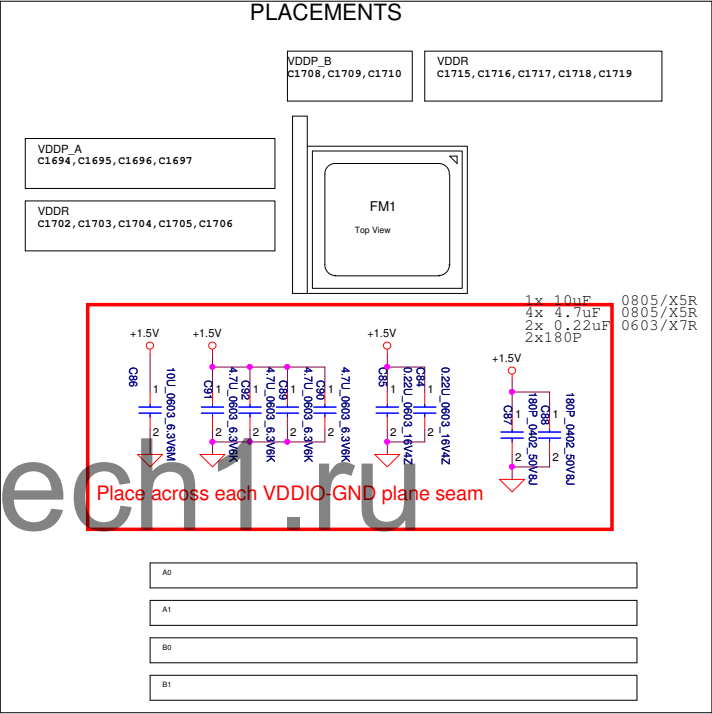
Place across each VDDIO-GND plane seam

A0

A1

B0

B1



VDDP_A
C1694, C1695, C1696, C1697

VDDP_B
C1708, C1709, C1710

VDDR
C1715, C1716, C1717, C1718, C1719

FM1
Top View

1x 10uF
4x 4.7uF
2x 0.22uF
2x 180pF
0805/X5R
0805/X5R
0603/X7R

+1.5V
C86 100u 0603, 6.3V6M
1 2

+1.5V
C91 4.7u 0603, 6.3V6K
C92 4.7u 0603, 6.3V6K
C93 4.7u 0603, 6.3V6K
C94 4.7u 0603, 6.3V6K
1 2

+1.5V
C95 0.22u 0603, 16V4Z
C97 0.22u 0603, 16V4Z
C98 0.22u 0603, 16V4Z
1 2

+1.5V
C97 180p 0402, 50V3J
C98 180p 0402, 50V3J
1 2

Place across each VDDIO-GND plane seam

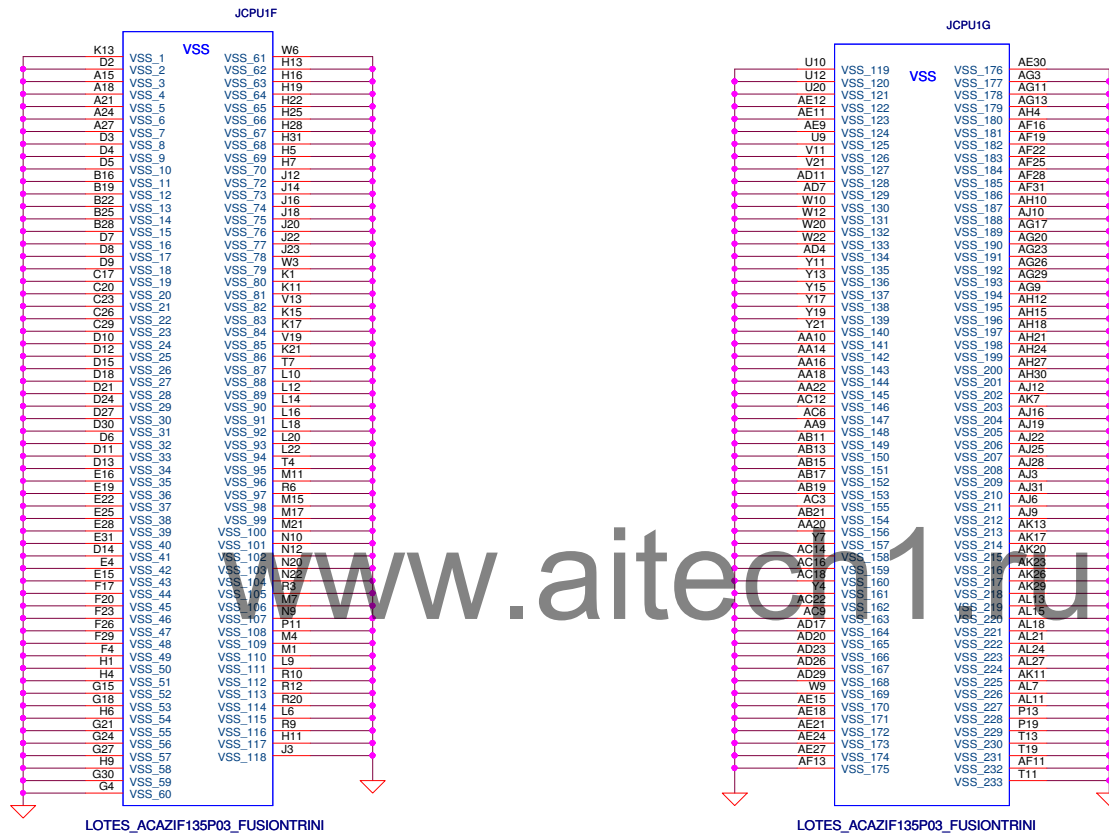
A0

A1

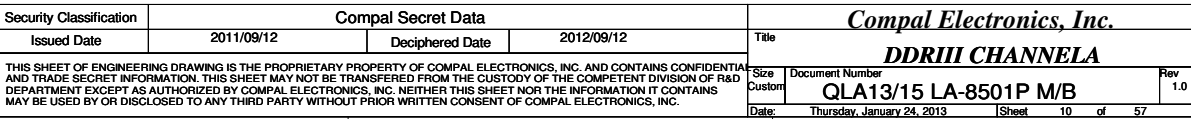
B0

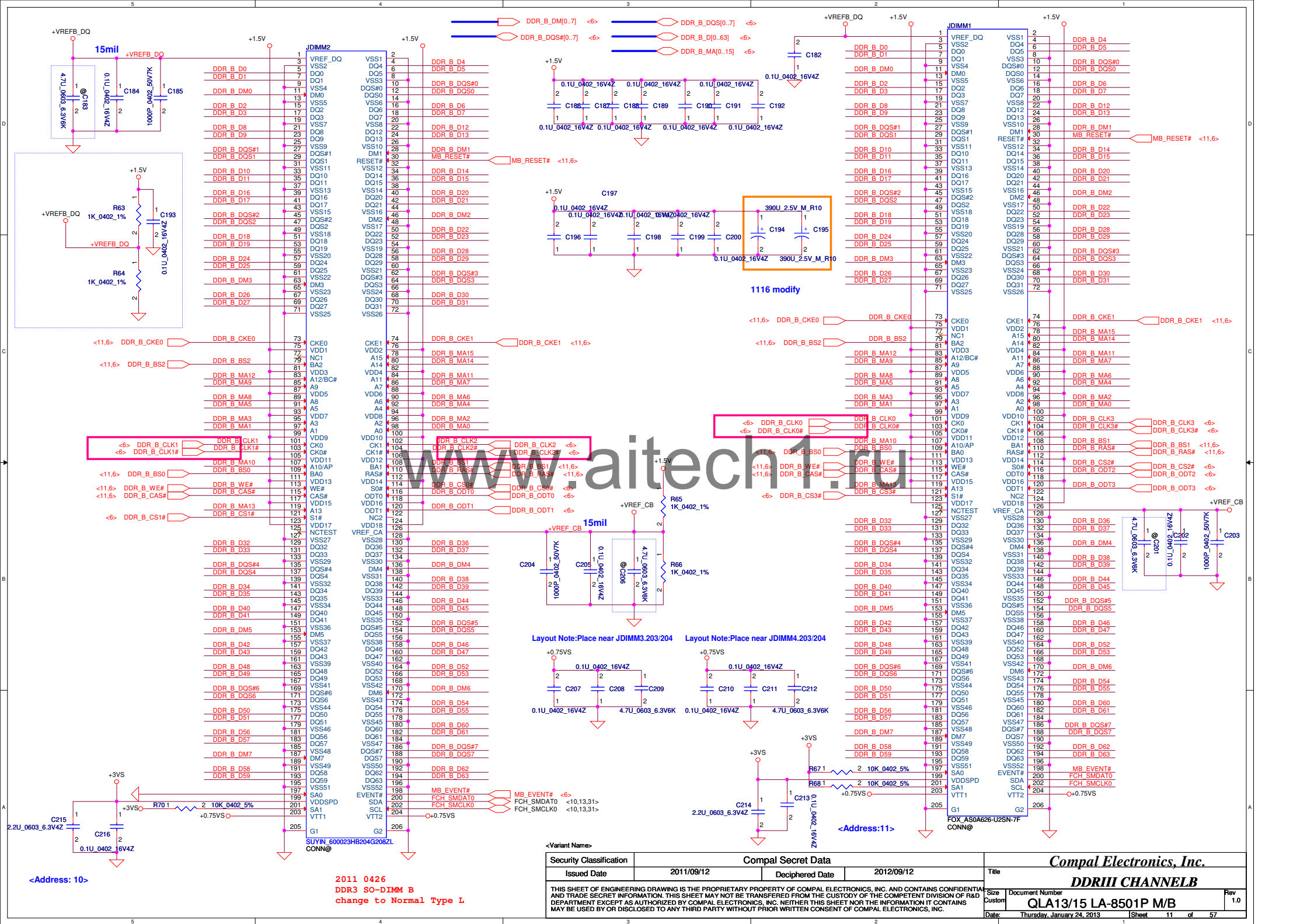
B1

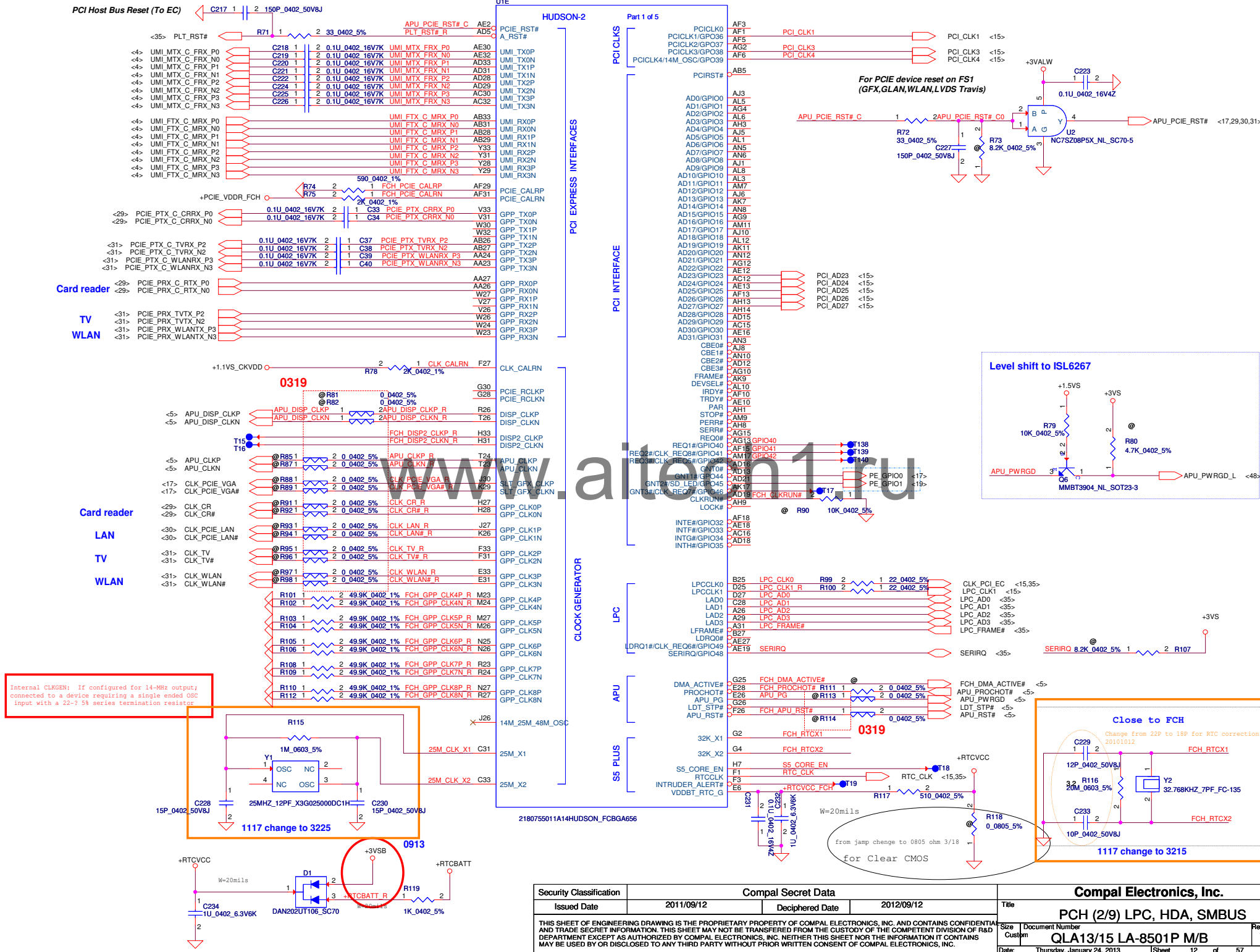
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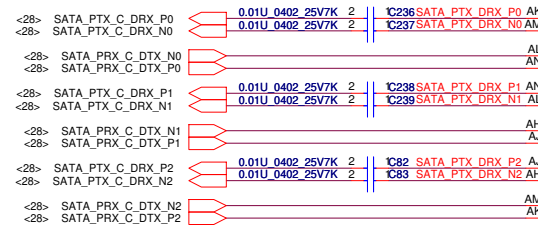




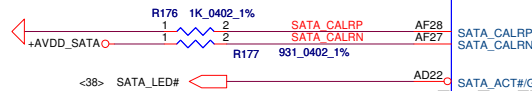
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HDD

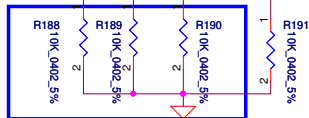
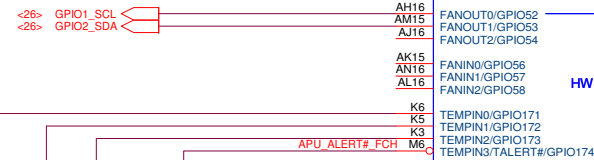
ODD



PUT SATA_CAL Resistors close to U600



Integrated Clock Mode: Left unconnected



HUDSON-2

Part 2 of 5

SD CARD

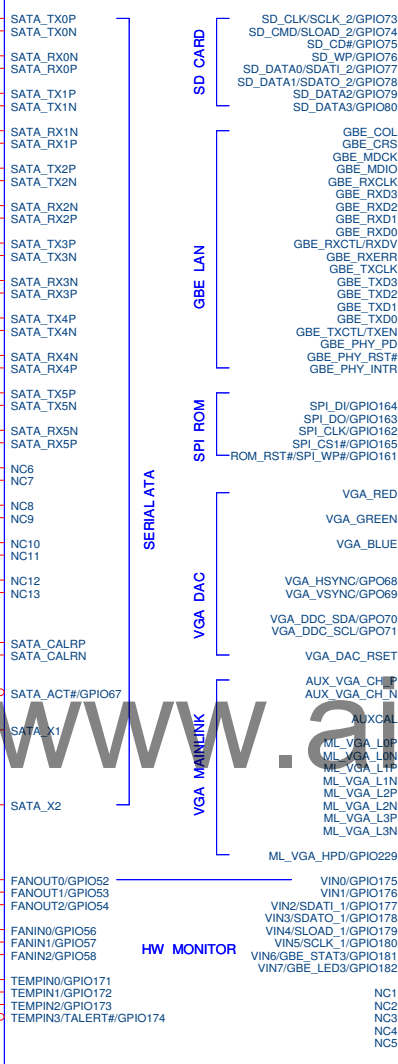
GBE LAN

SPI ROM

VGA DAC

VGA MAINLINK

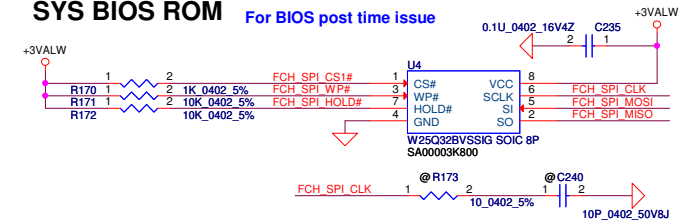
HW MONITOR



2180755011A14HUDSON_FCBGA656

SYS BIOS ROM

For BIOS post time issue



0319

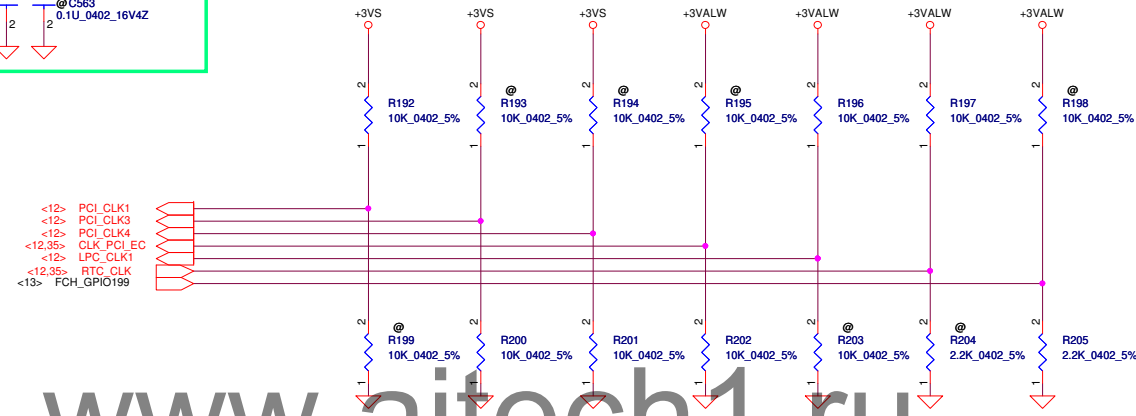
Use as GPIO or configure for one of the following options if not used.

- 10-KΩ 5% pull-up resistor to +3.3V_{S5}.
- 10-KΩ 5% pull-down resistor.

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STRAP PINS

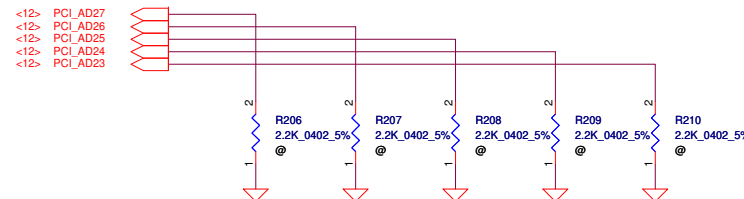
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	FCH_GPIO199	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



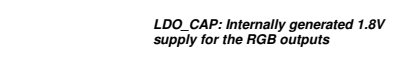
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

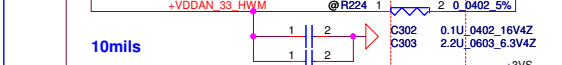
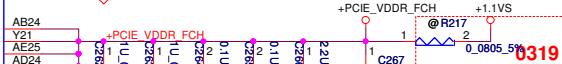
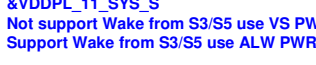
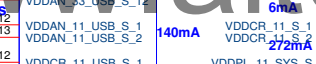
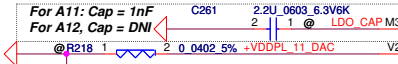
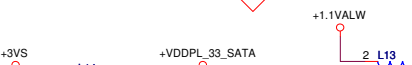
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal REFCLK termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISEMBLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	RESERVED	Inverted REFCLK termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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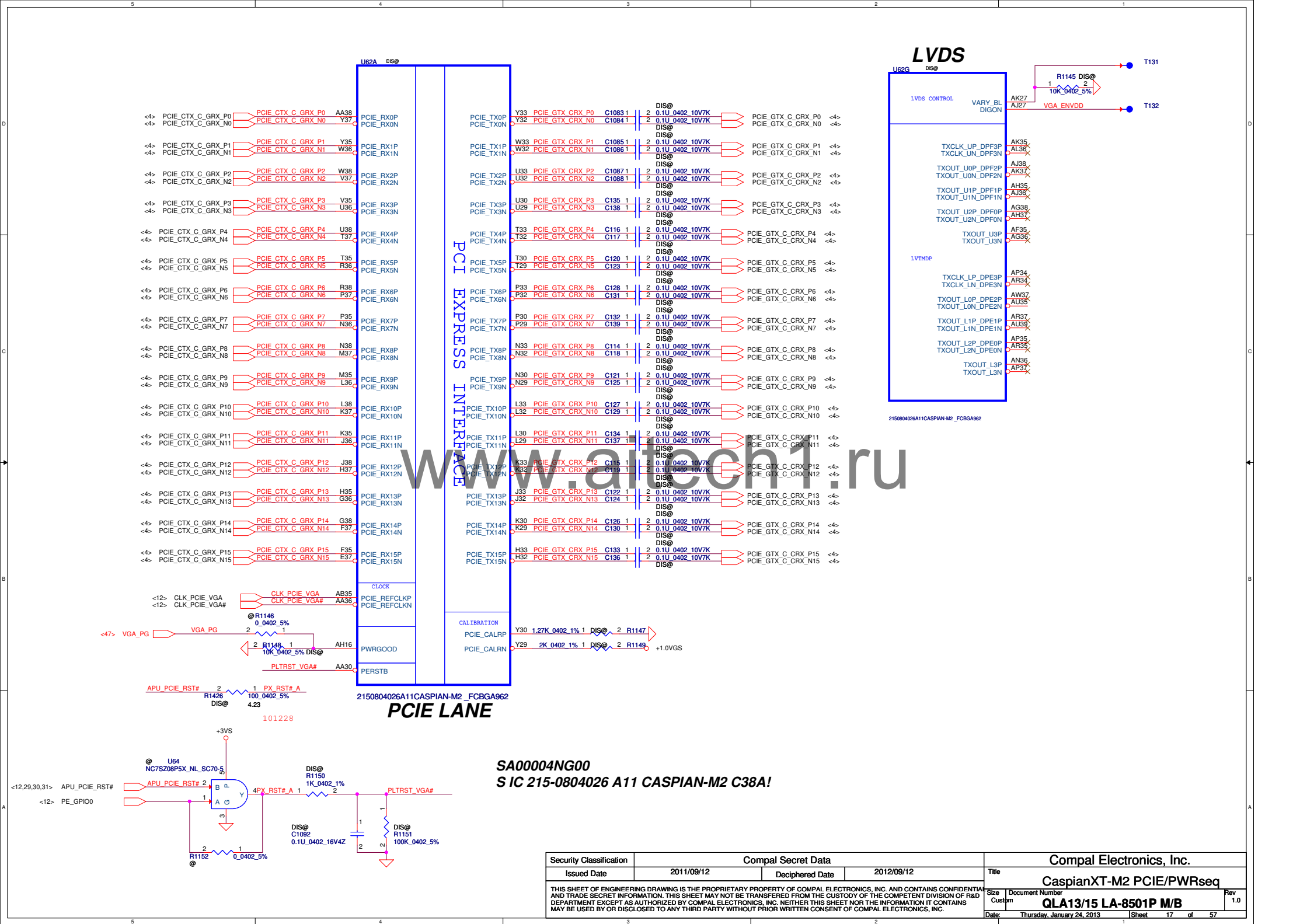
For Hudsonz, connect to GND:DZ@

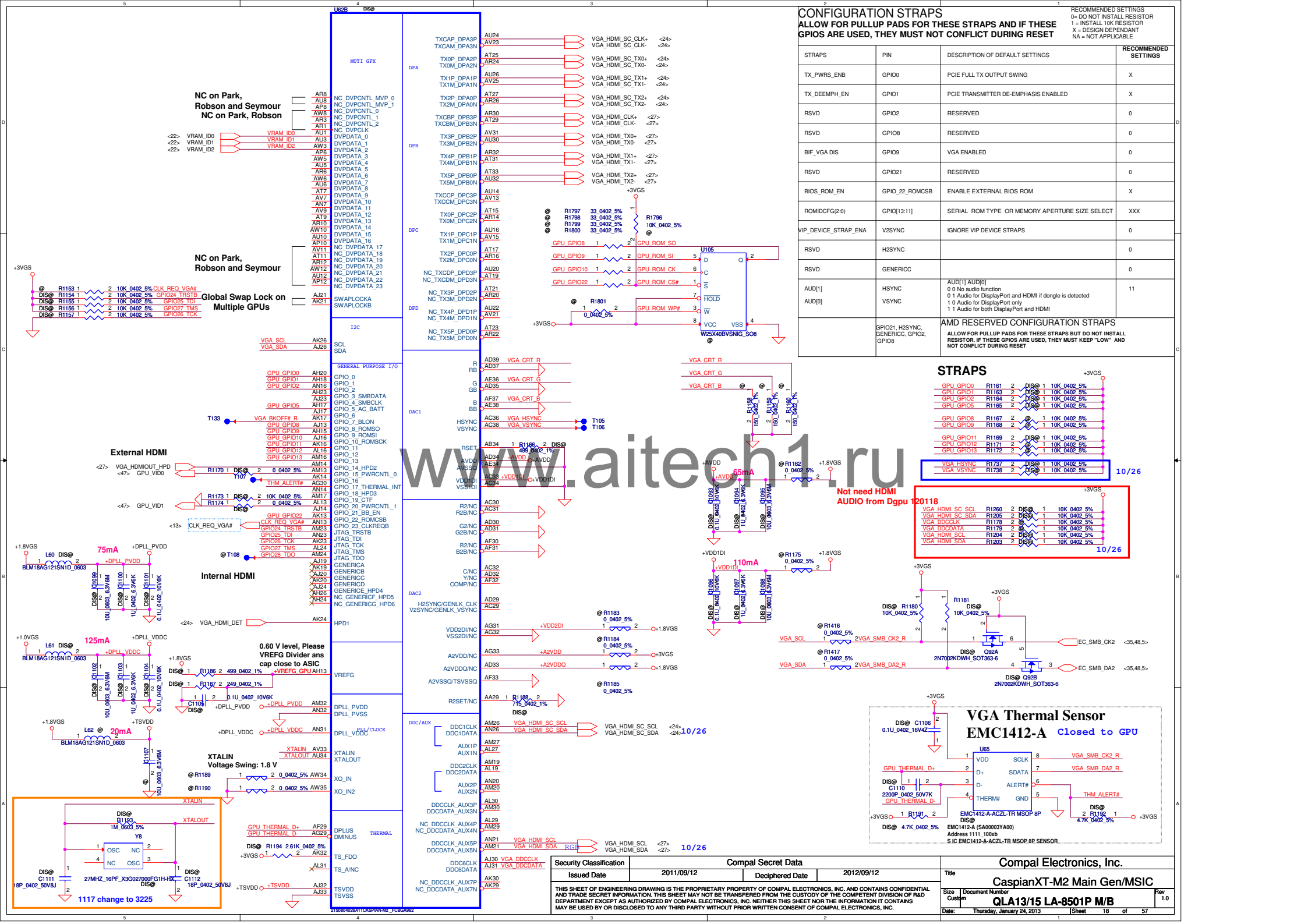


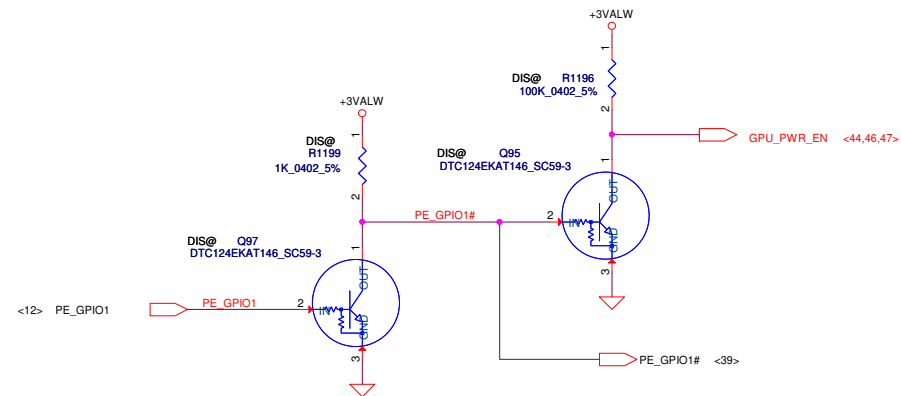
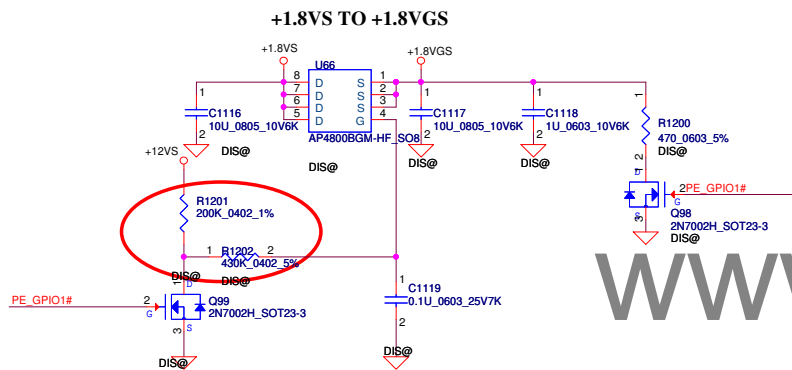
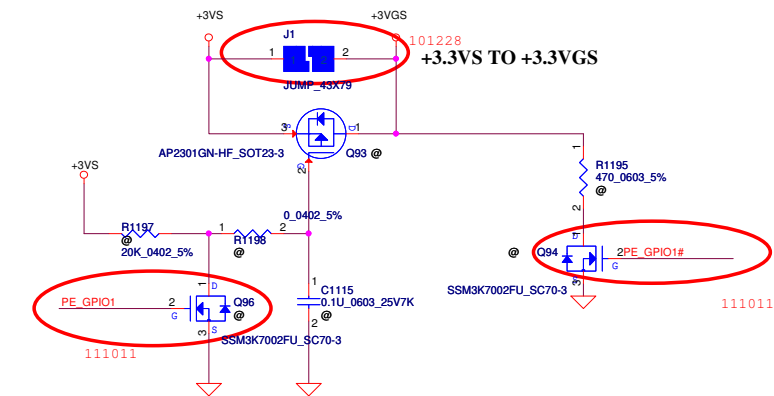
Bead for HWM



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				Size	Document Number	Rev			
				Custom	QLA13/15 LA-8501P M/B				
				Date:	Thursday, January 24, 2013	Sheet	16	of	57

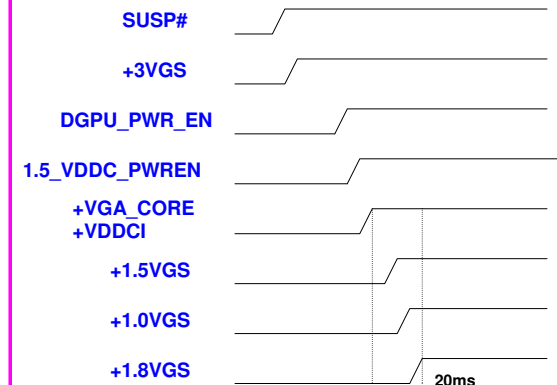




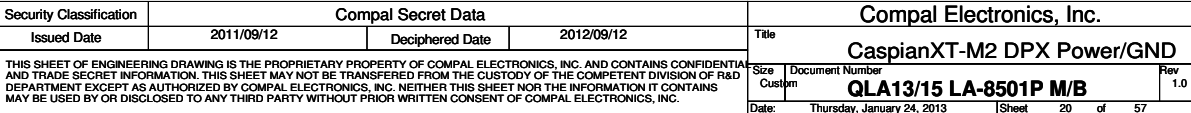


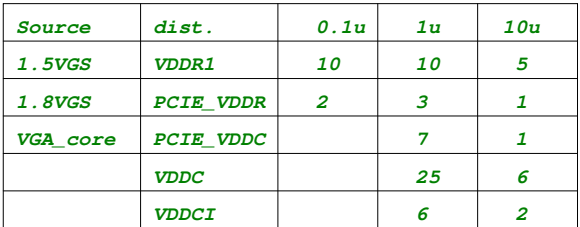
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Power Sequence of Whistler and Seymour

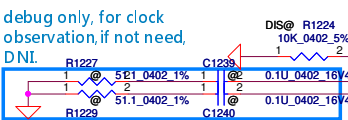
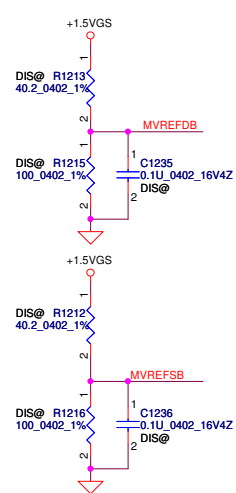


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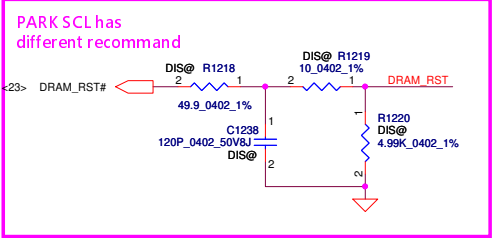




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<23> M_DQSB[7..0] M_DQSB[7..0]
<23> M_DQSB#7..0 M_DQSB#7..0



Route 50ohms single-ended/100ohm diff and keep short



U6B0 DS0

MEMORY INTERFACE B

MEMORY INTERFACE B

MEMORY INTERFACE B

MEMORY INTERFACE B

MEMORY INTERFACE B

MEMORY INTERFACE B

MEMORY INTERFACE B

MEMORY INTERFACE B

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MEMORY INTERFACE B

U6B0 DS0

DDR2

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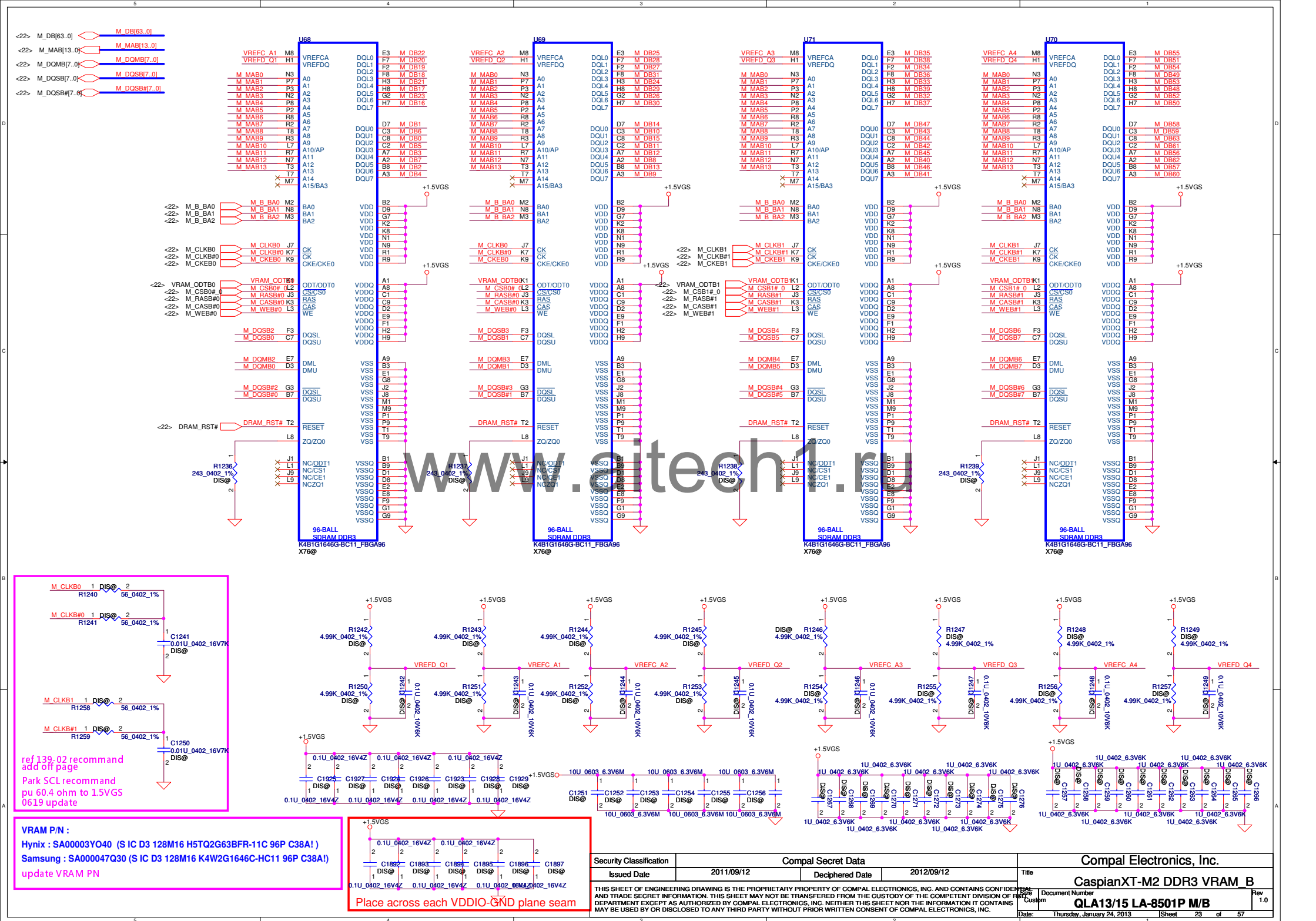
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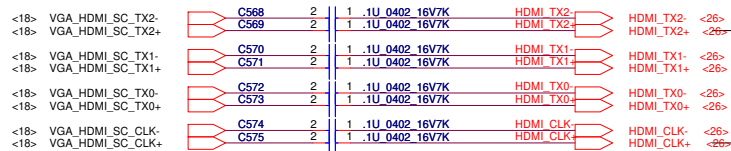
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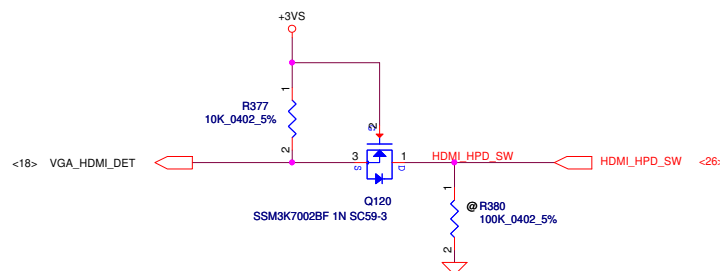
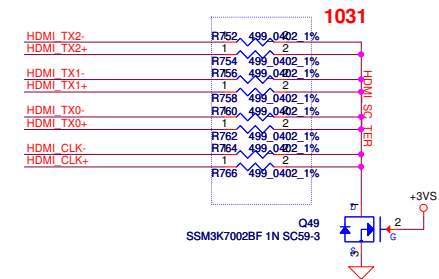
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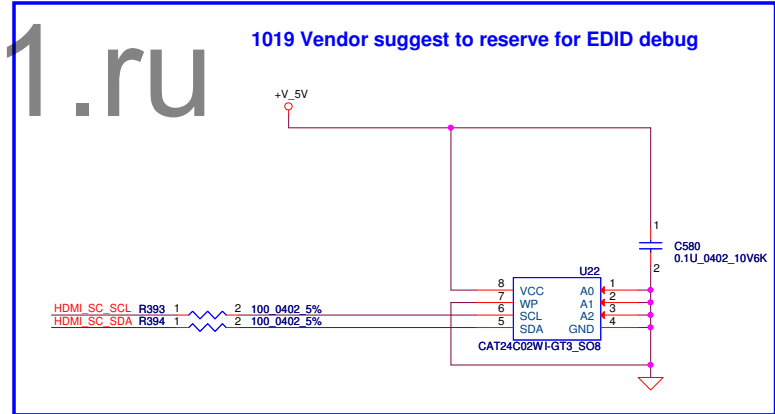
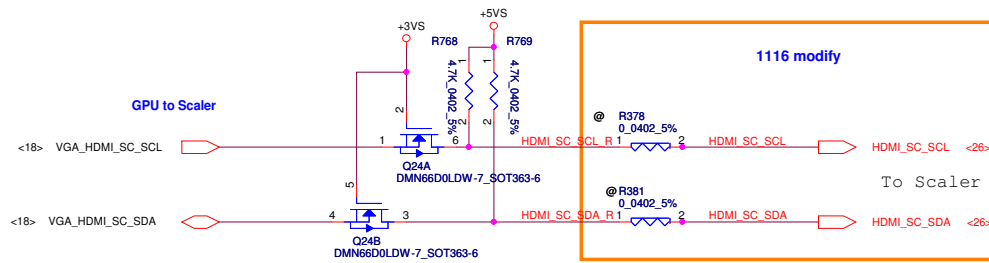




To Scaler

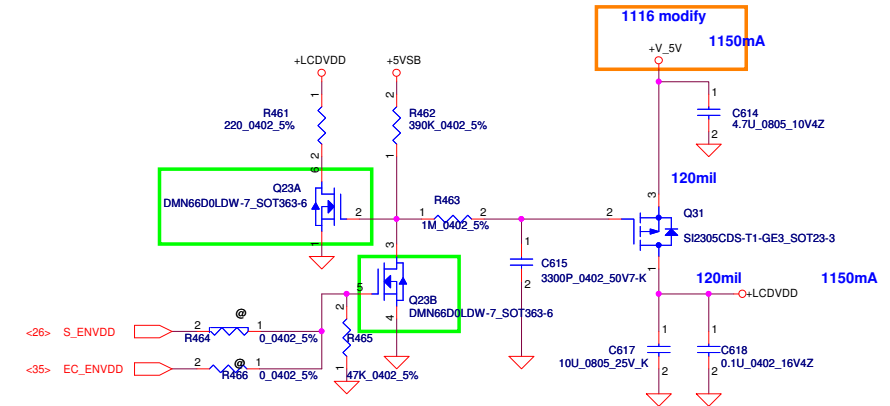


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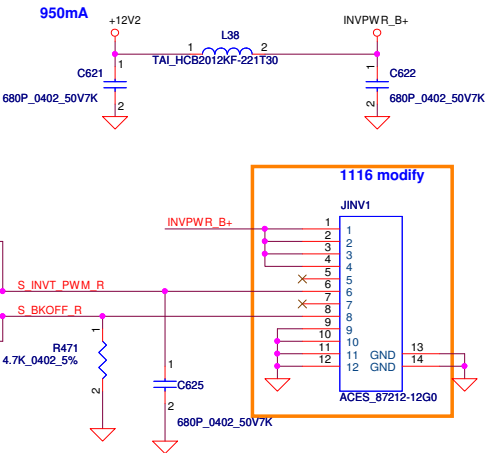


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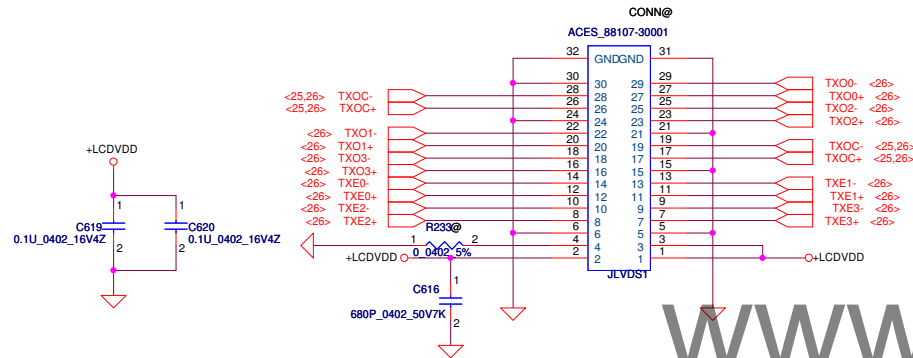
LVDS POWER



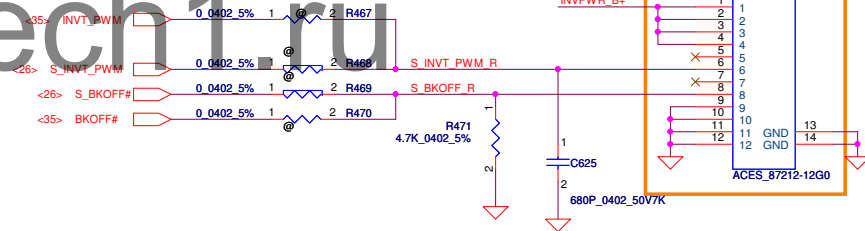
Converter



LVDS CONN

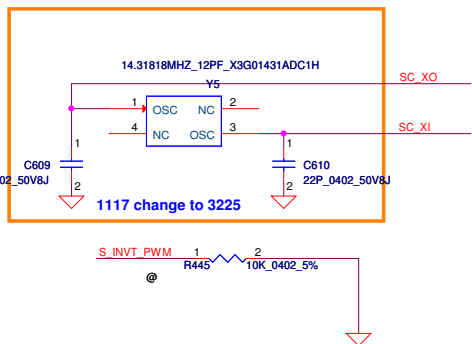
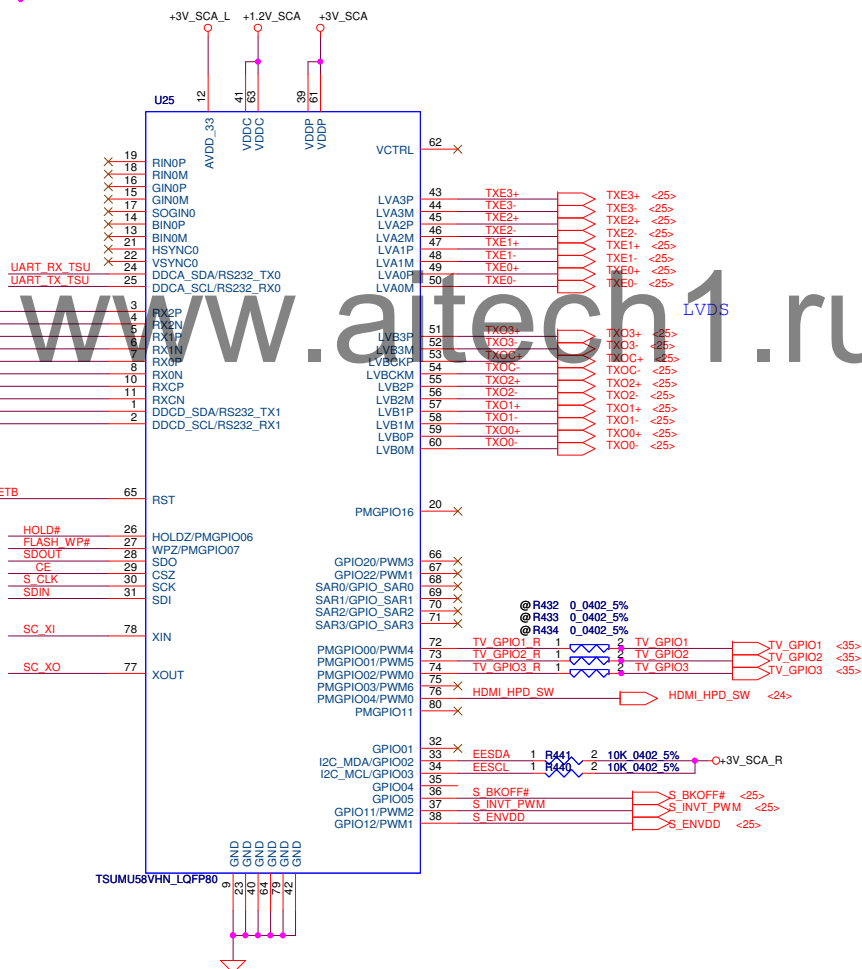
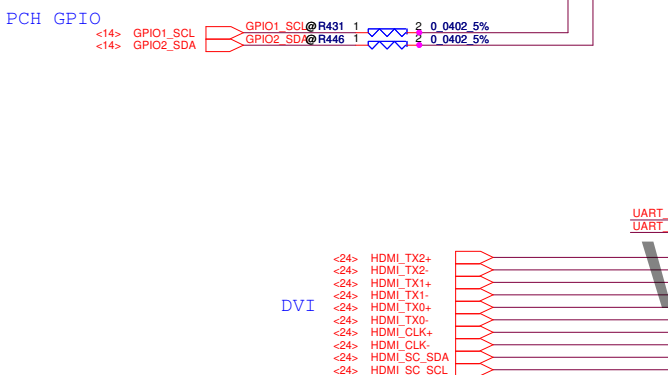
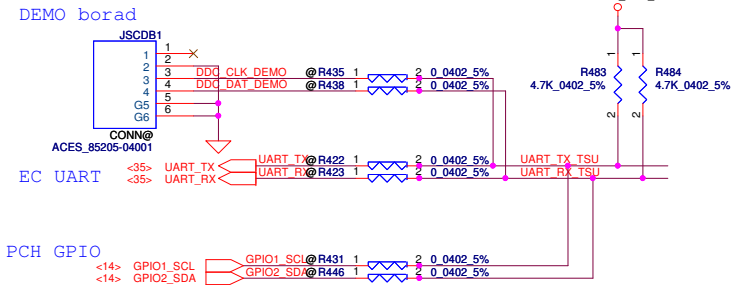
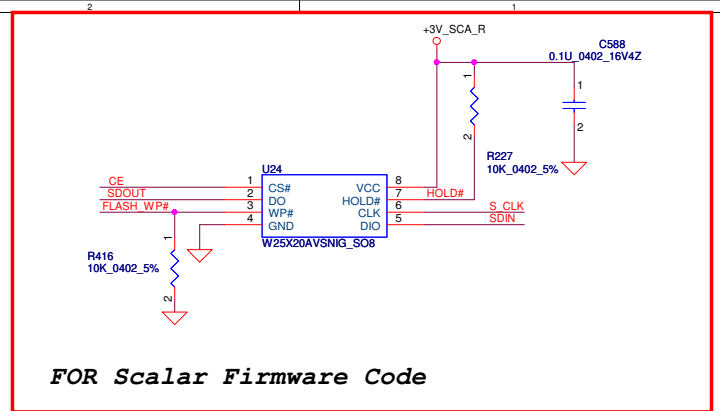
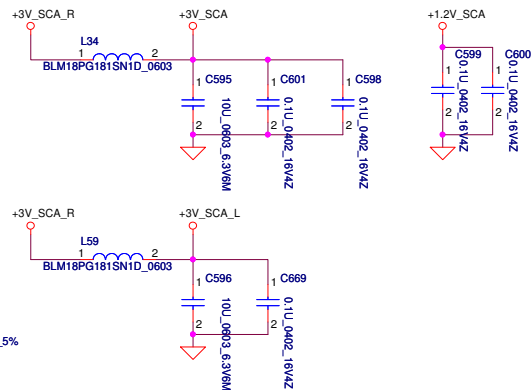
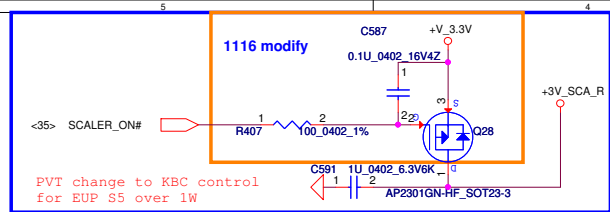


INVT_PWM: scalar-> converter
BKOFF#: scalar-> converter



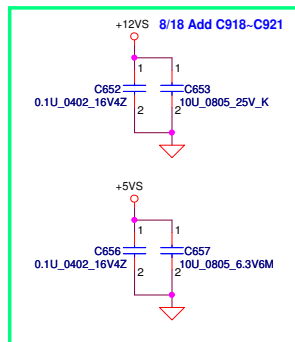
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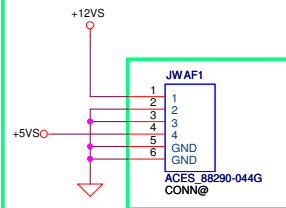


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HDD POWER Conn



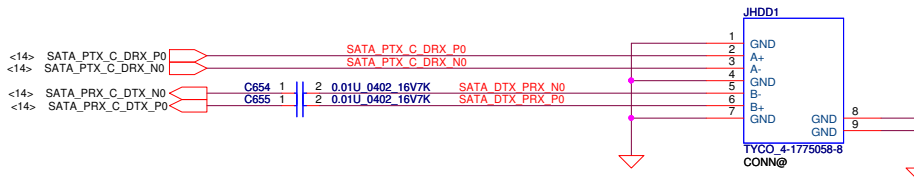
HDD



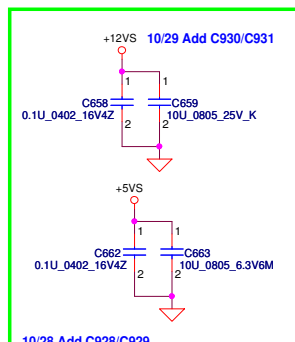
12/6 Change footprint of JWF1 from SP02000AO00 to SP02000EB00

Layout Note: Place C918/C919/C920/C921 close to JWF1

SATA HDD Conn.

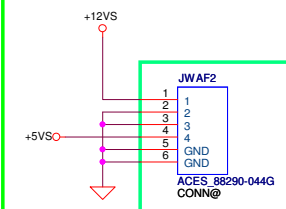


ODD POWER Conn



10/28 Add C928/C929

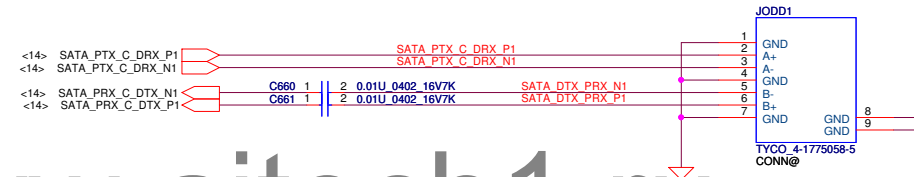
Layout Note: Place C928/C929 close to JWF2



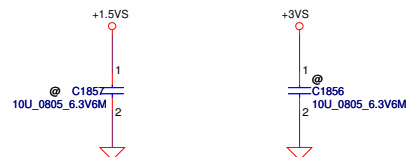
12/6 Change footprint of JWF1 from SP02000AO00 to SP02000EB00

ODD

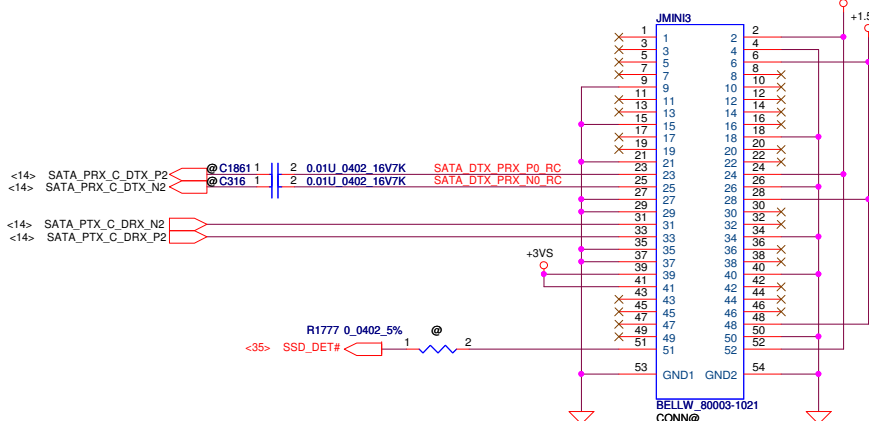
SATA ODD Conn.



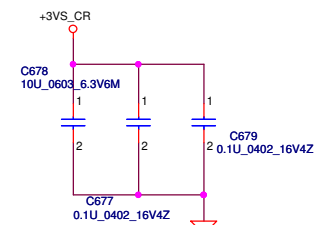
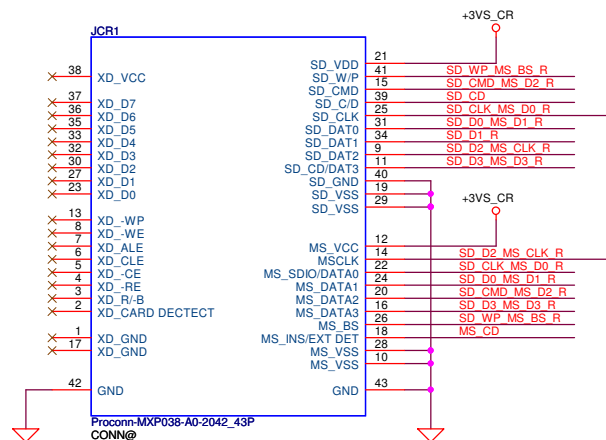
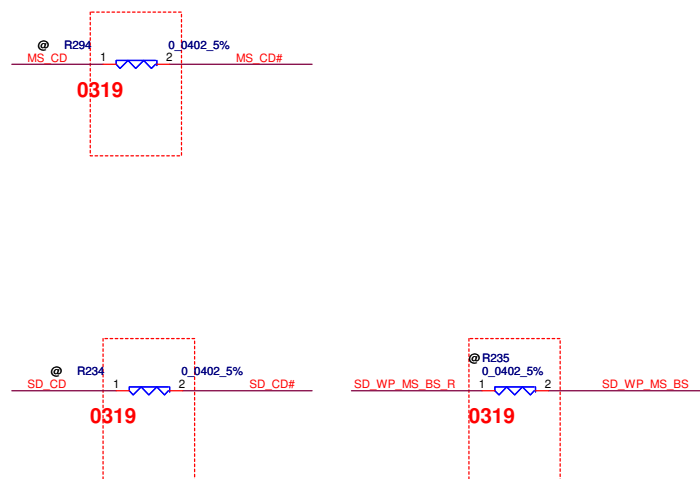
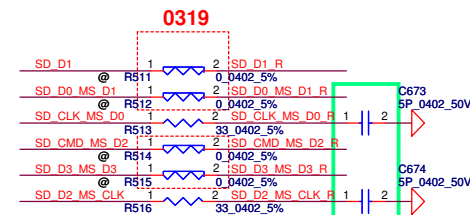
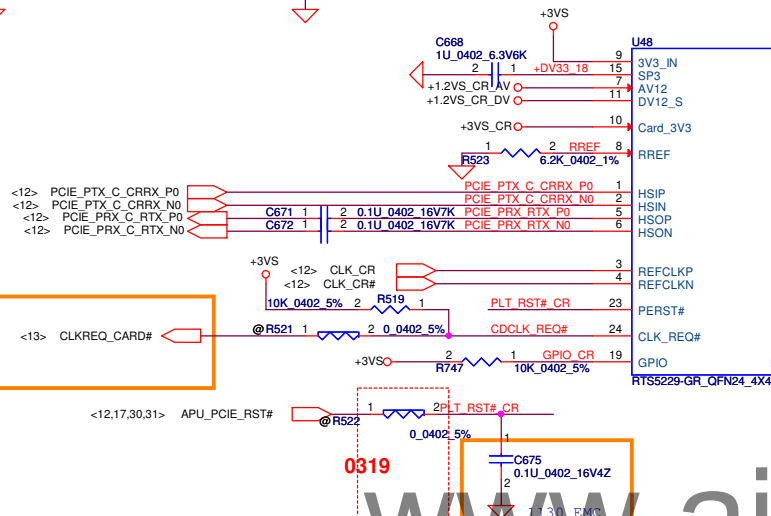
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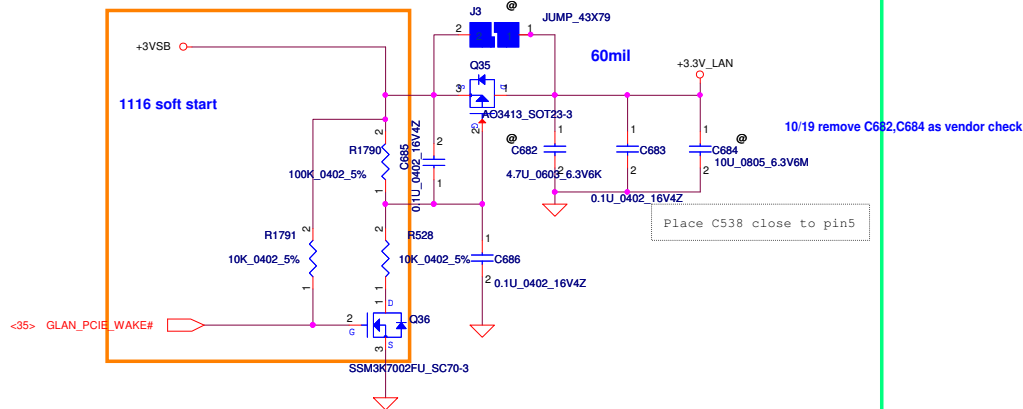
MINI SSD Conn.



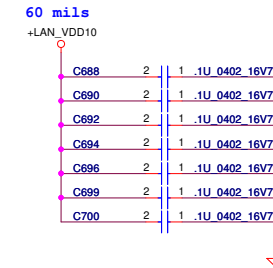
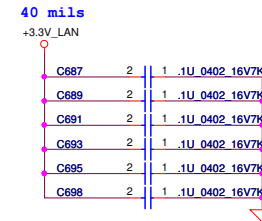
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				Rev	1.0

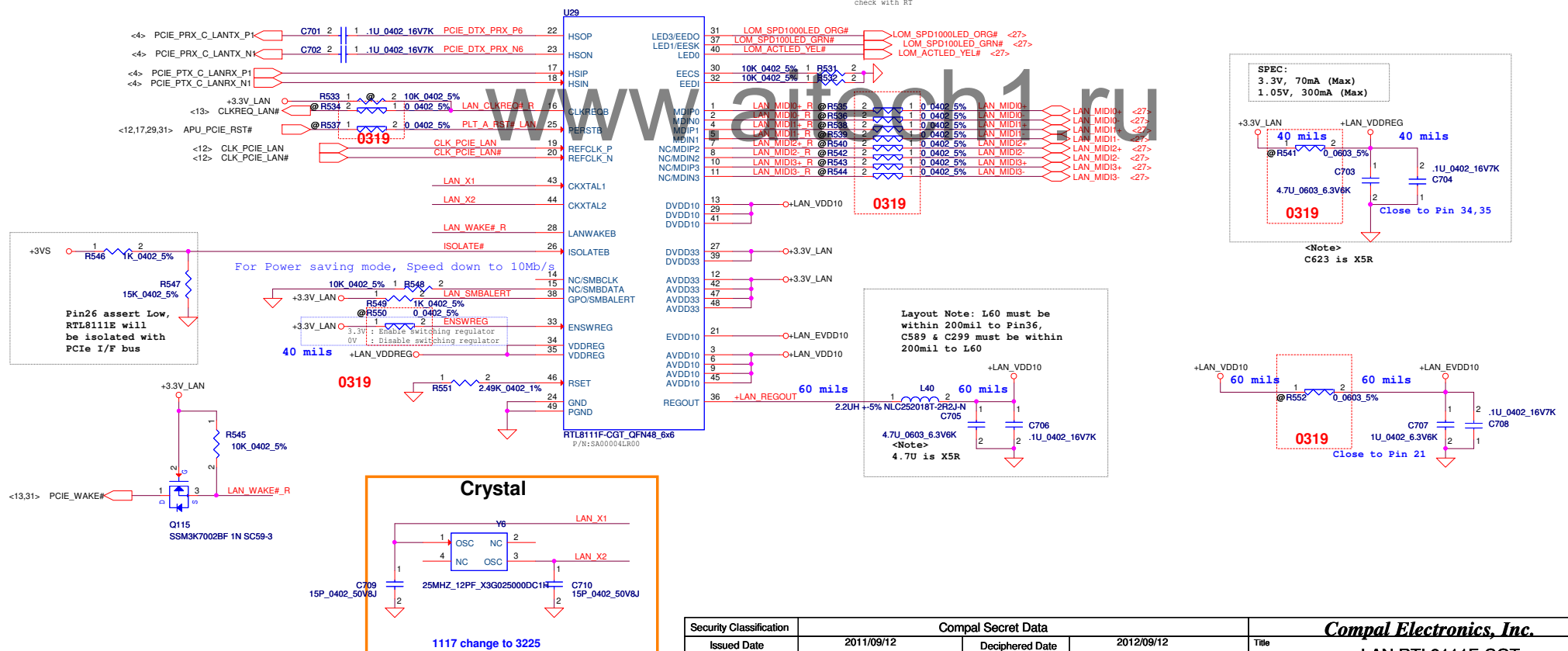


Power (Decoupling Cap.)



C625, C610, C617, C626, C621, C604 close to Pin 12,27,39,42,47,48, respectively

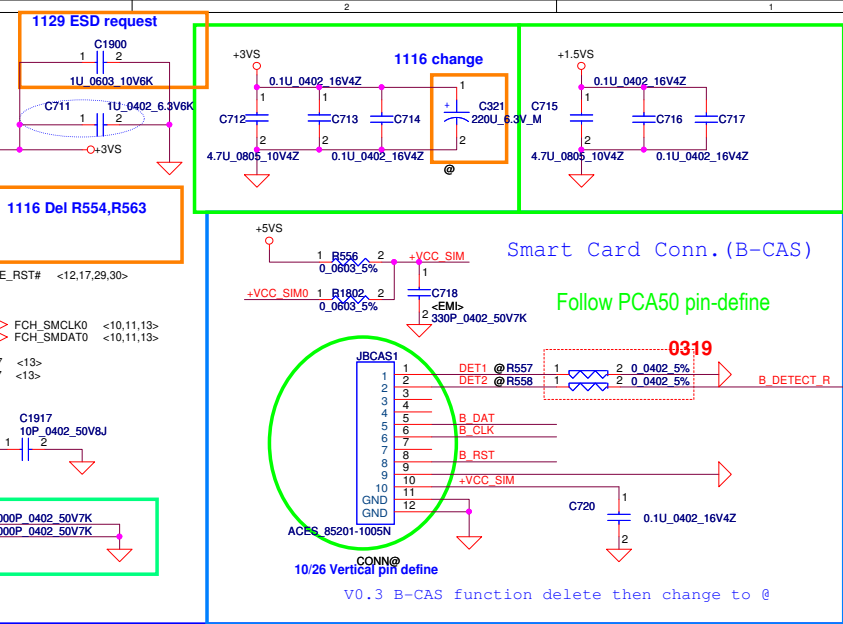
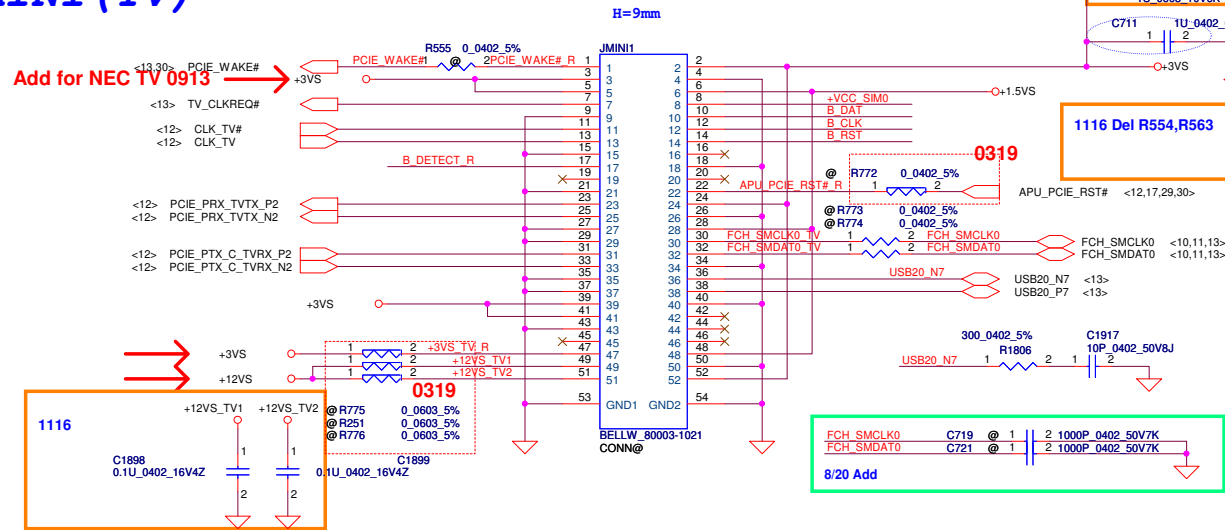
C615, C614, C622, C620, C616, C611, C624 close to pin 3,6,9,13,29,41,45, respectively



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				QLA13/15 LA-8501P M/B	1.0
				Date: Thursday, January 24, 2013	Sheet 30 of 57

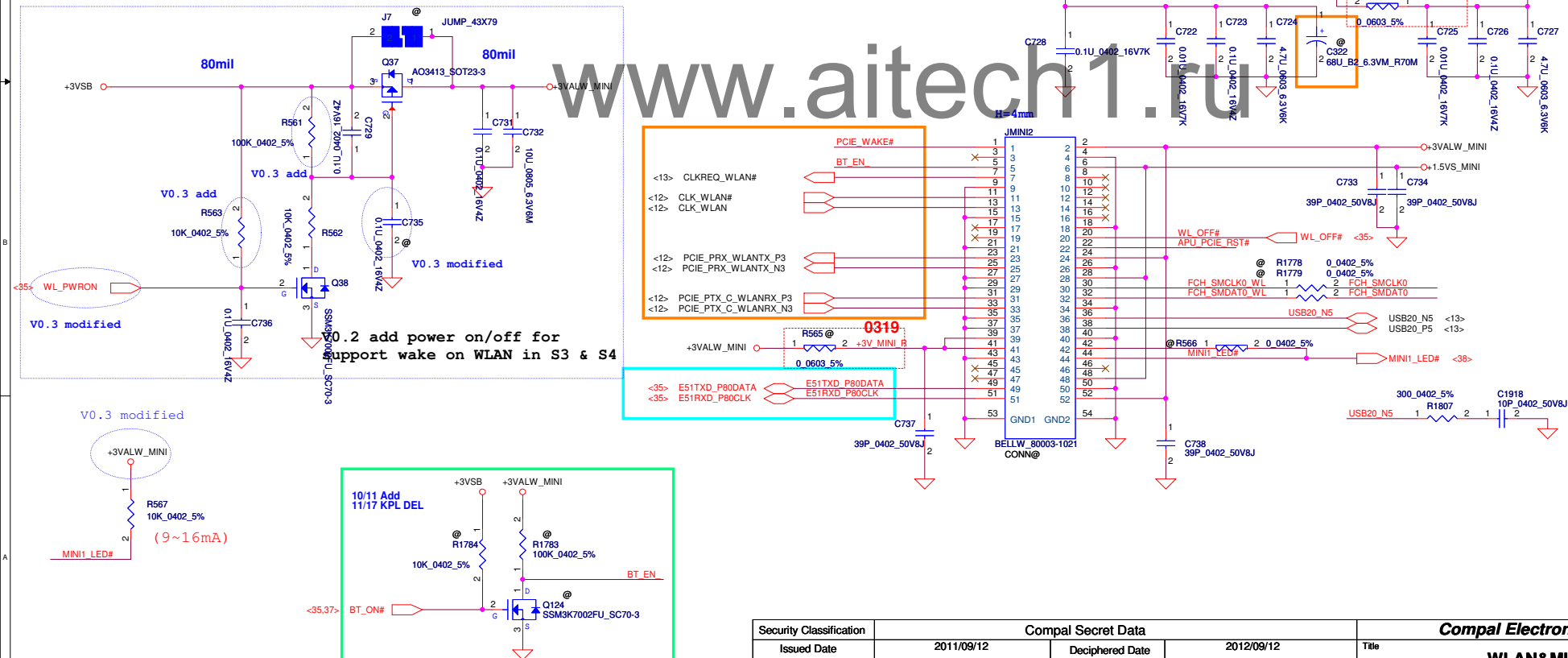
MINI (TV)

Mini Card Slot 1---TV tuner Current: 3.3 : 2750mA, 1.5: 500mA



WLAN

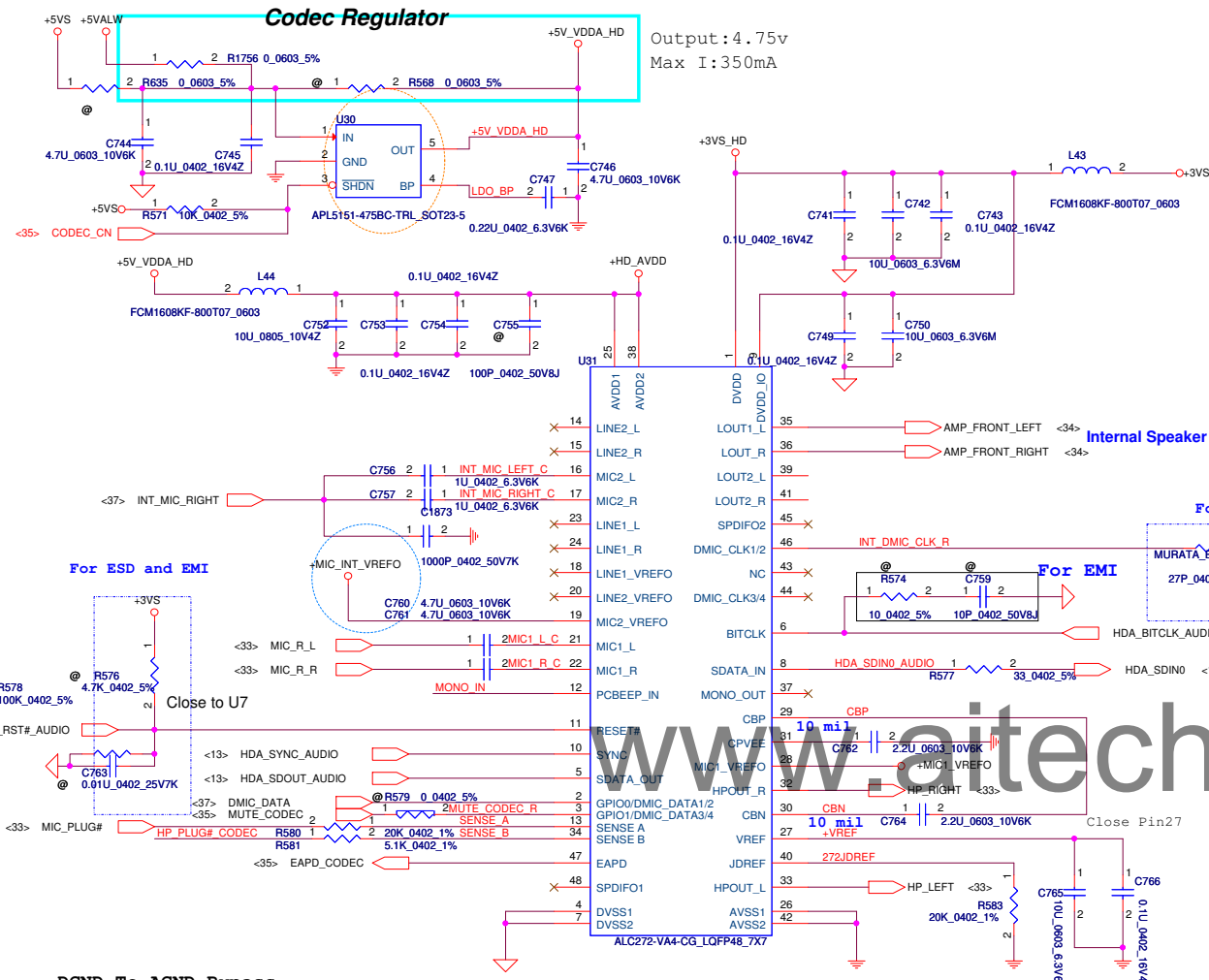
Mini Card Slot 1--- WLAN Current: 3.3 : 800mA,



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Codec Regulator

Output: 4.75v
Max I: 350mA



For ESD and EMI

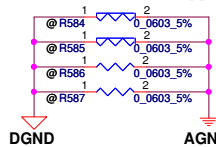
Internal Speaker

For EMI

For EMI

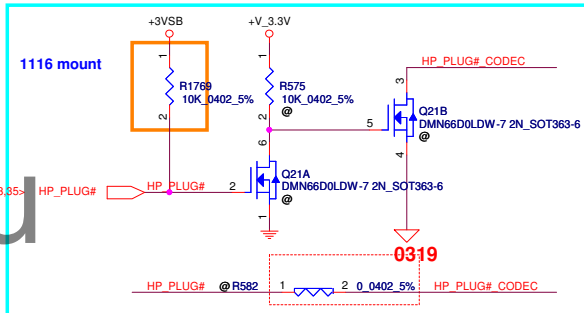
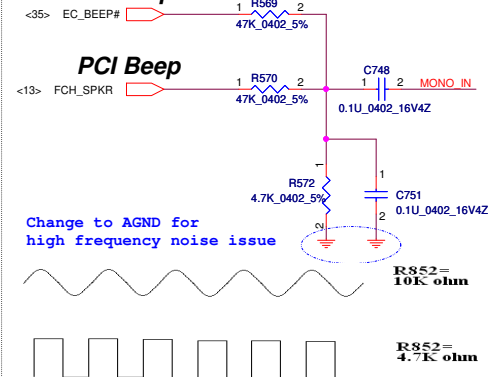
Close Pin27

DGND To AGND Bypass



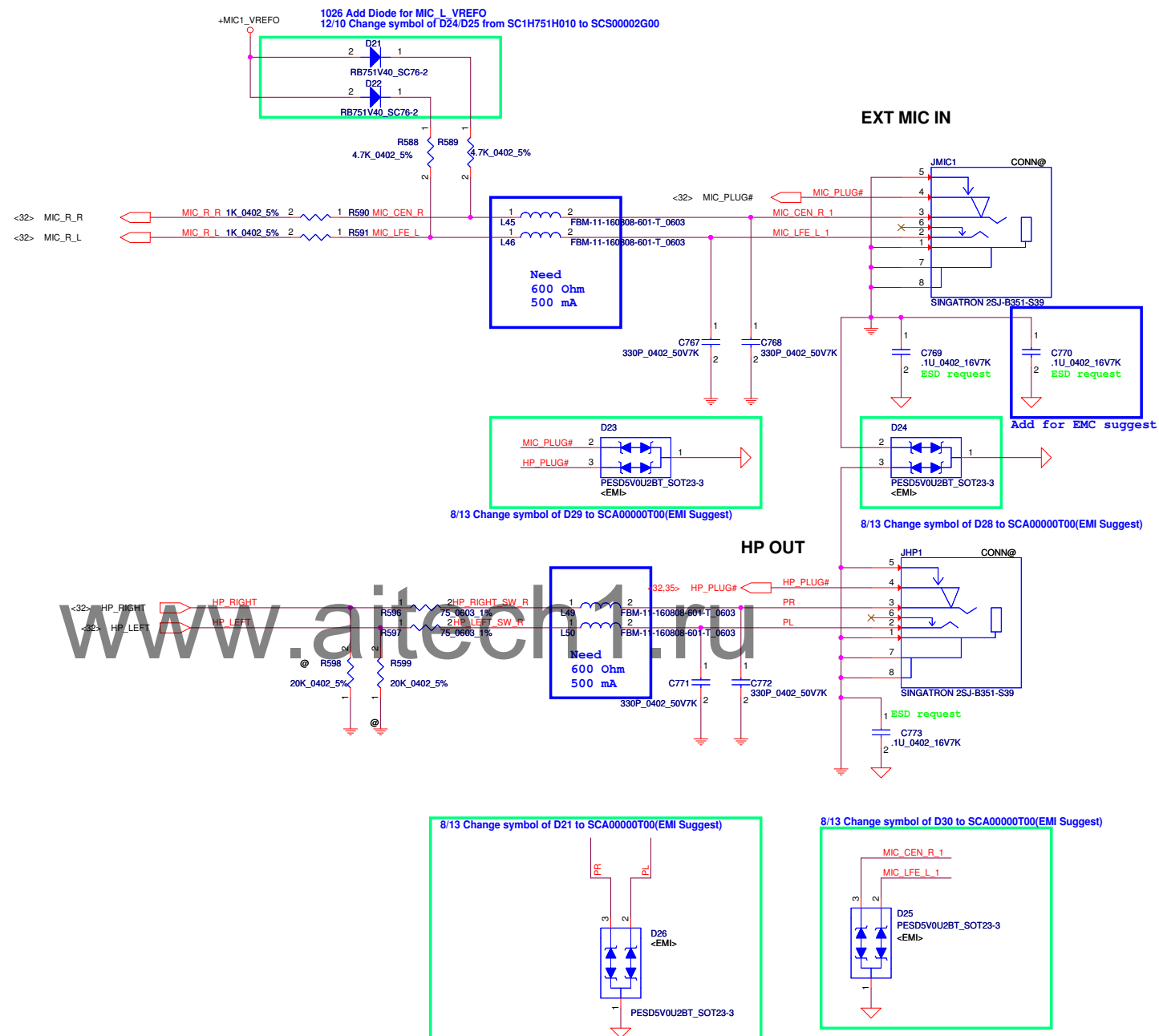
EC Beep

Beep sound



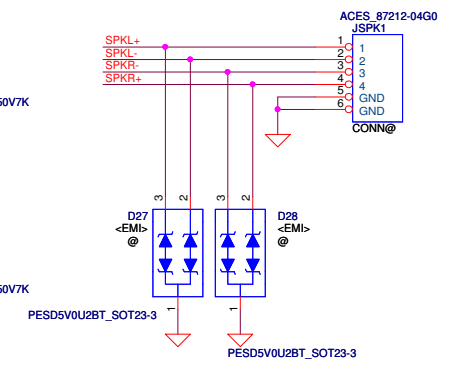
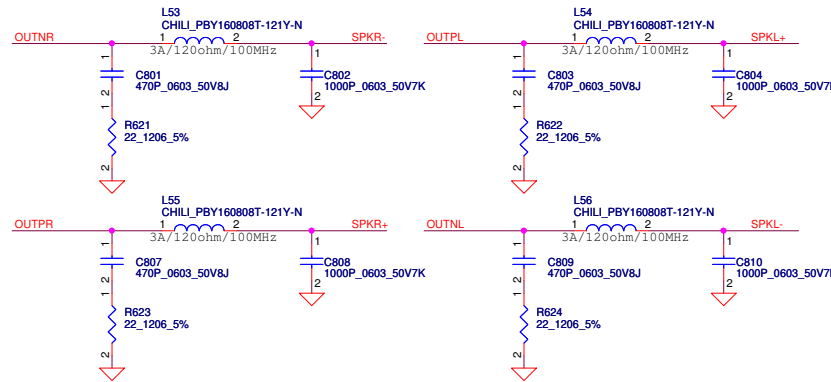
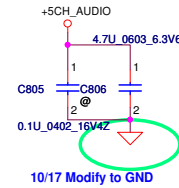
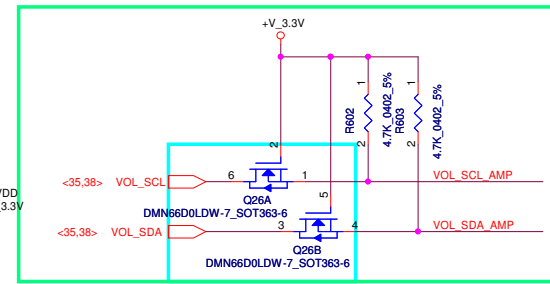
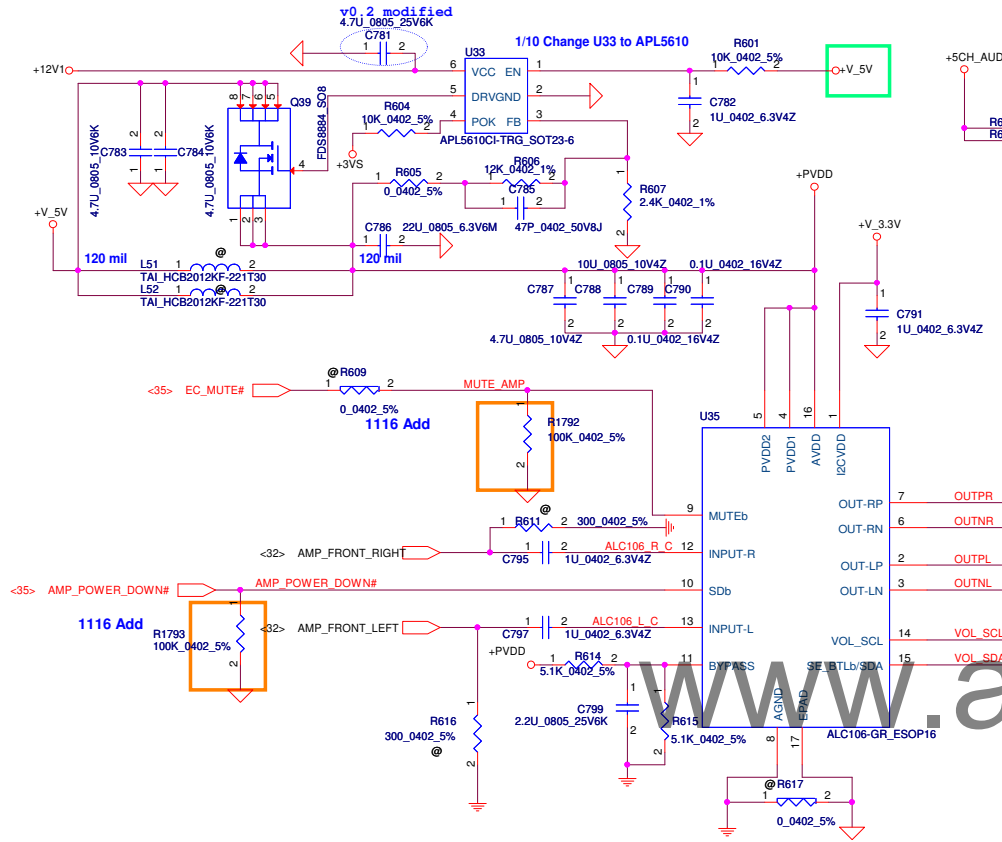
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	LOUT2 (PIN 39, 41)
	20K	MIC1 (PIN 21, 22)
	10K	LINE1 (PIN 23, 24)
	5.1K	LOUT1 (PIN 35,36)
SENSE B	39.2K	LINE2 (PIN 14, 15)
	20K	MIC2 (PIN 16, 17)
	10K	
	5.1K	HP-OUT (PIN 32,33)

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				Date	Thursday, January 24, 2013
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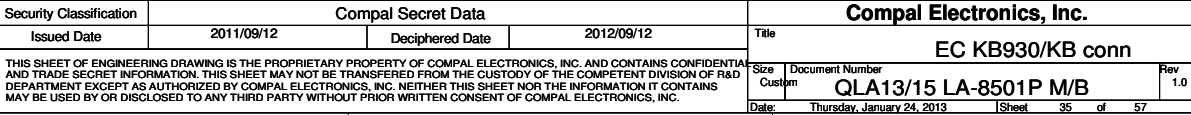


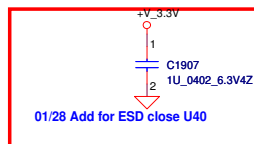
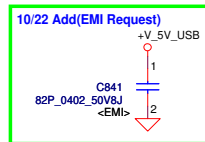
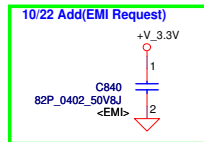
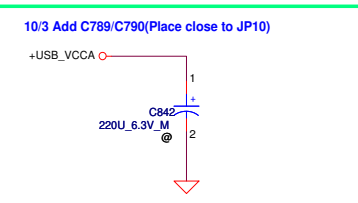
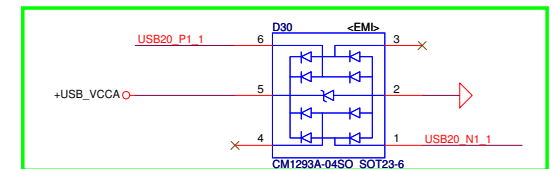
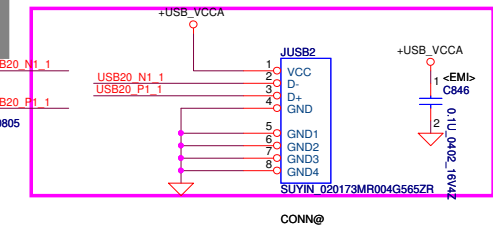
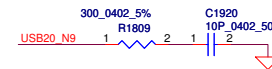
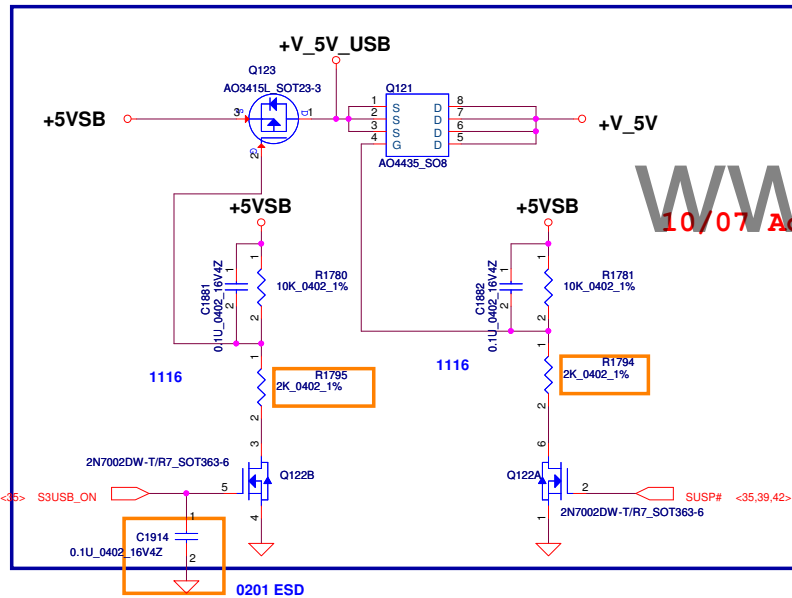
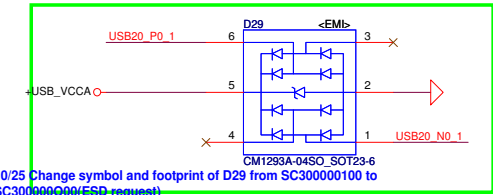
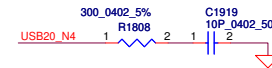
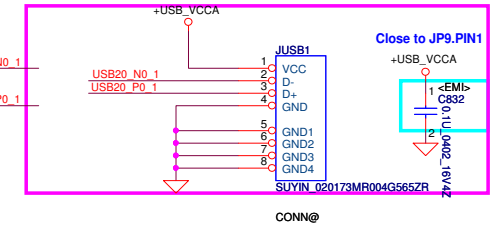
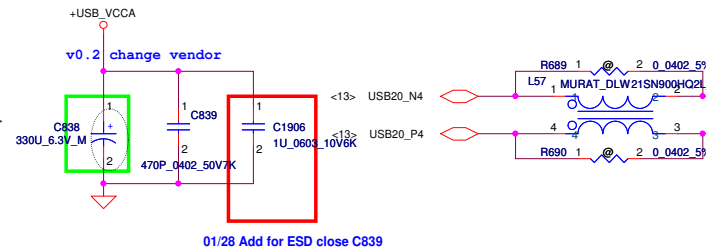
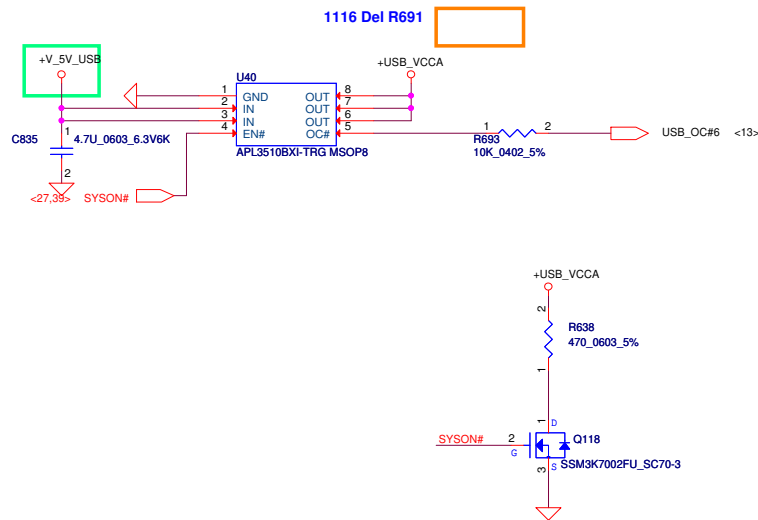
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Vo=0.8 (1+R606/R607)
Output:4.8V
Max I:7.5A



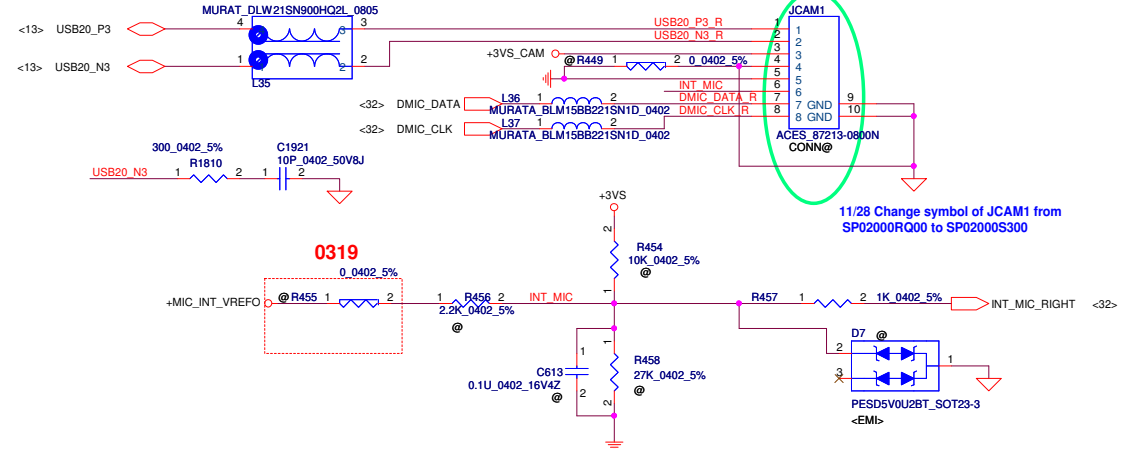
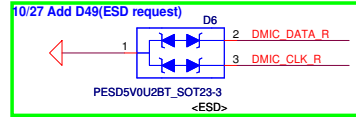
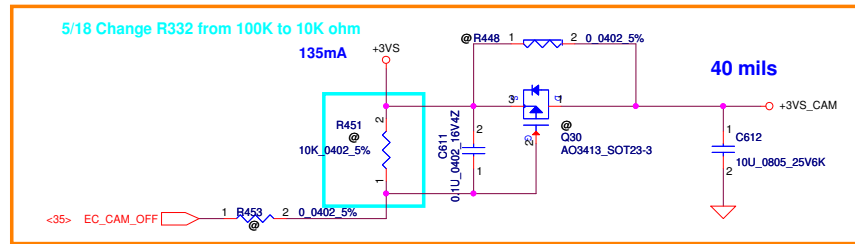
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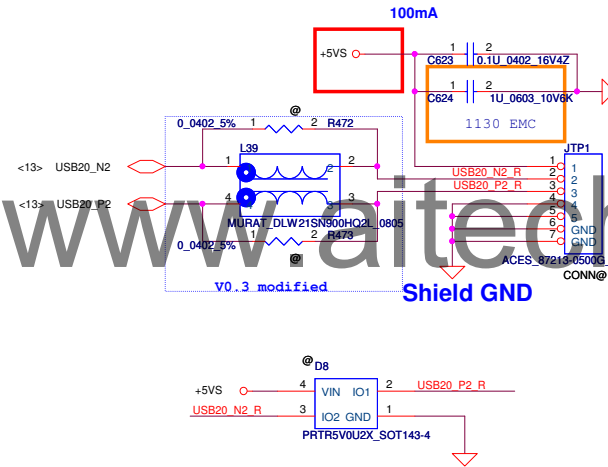
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/09/12	Deciphered Date	2012/09/12	Title
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WebCam+Digital Mic

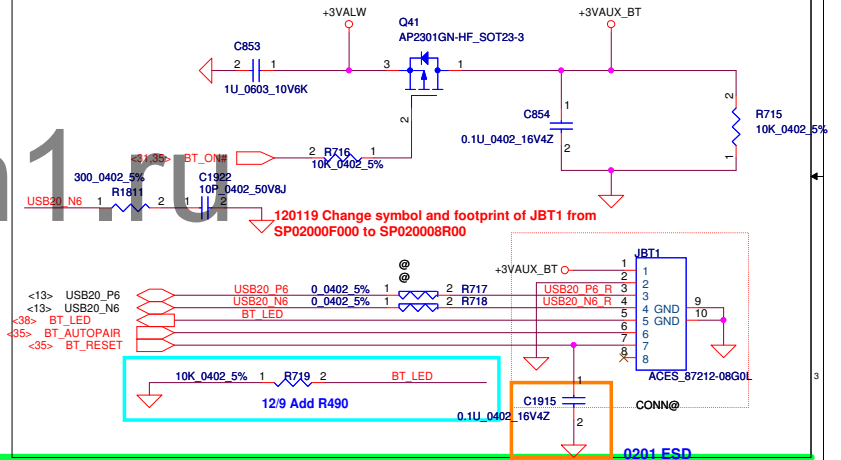


Touch Panel

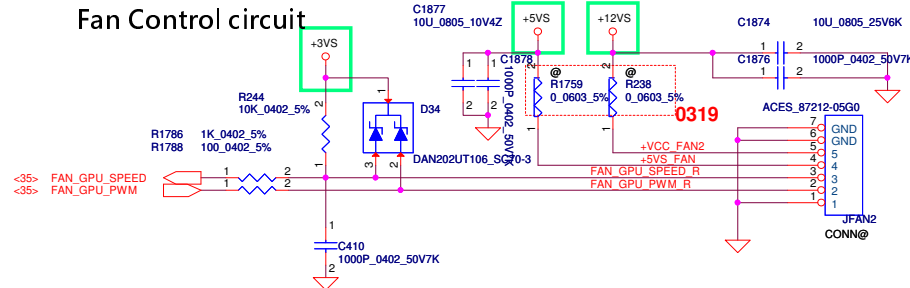
PVT change from alw to vs for EUP.



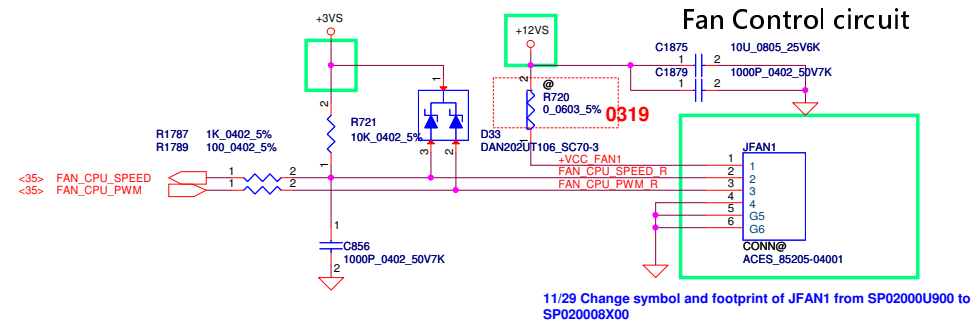
BT Connector



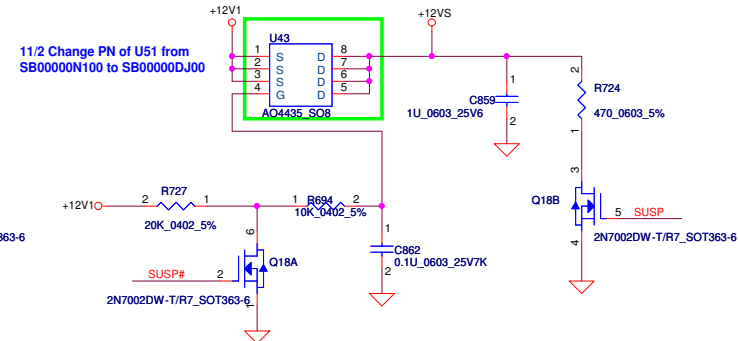
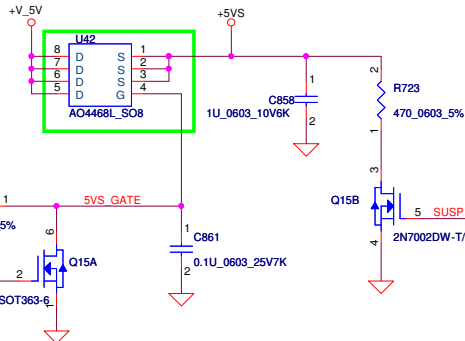
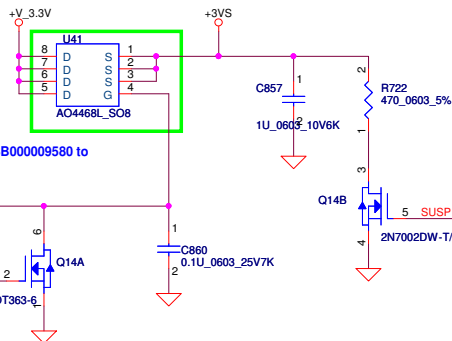
Fan Control circuit



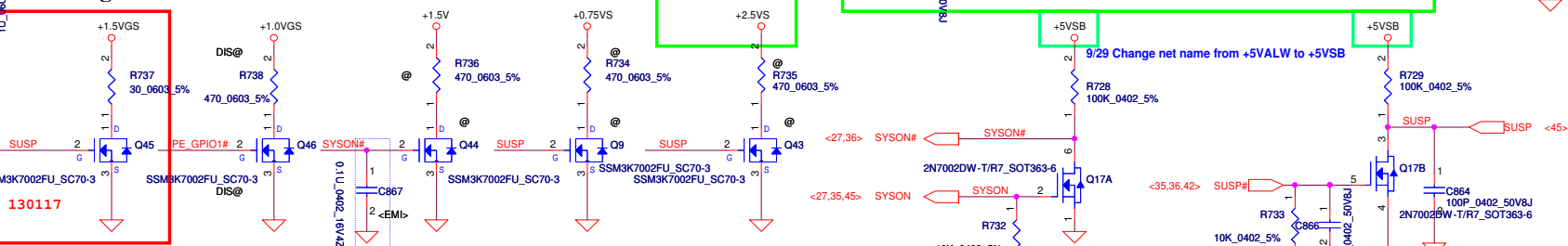
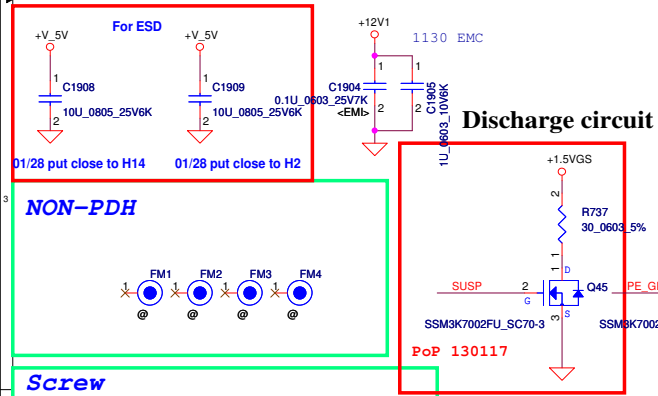
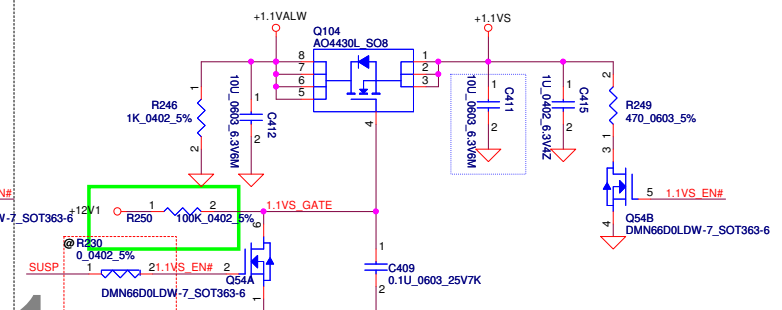
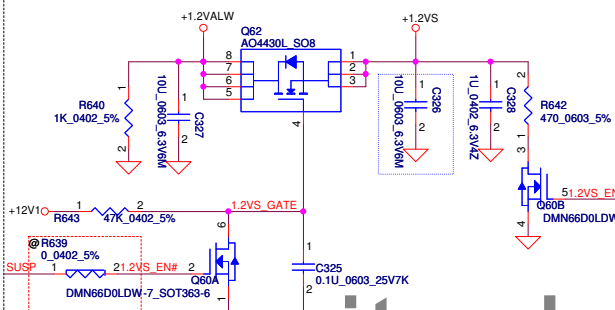
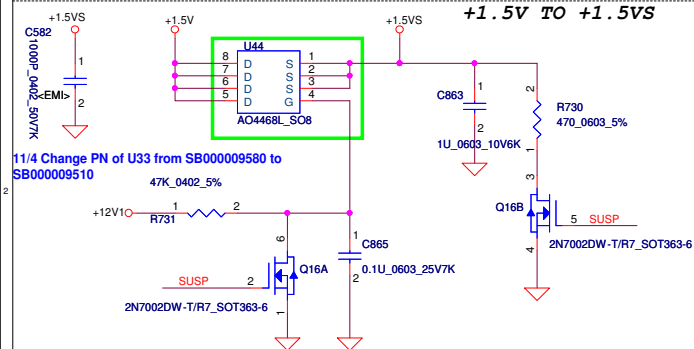
Fan Control circuit



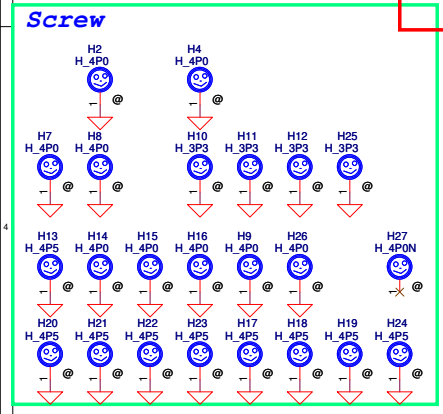
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						Size Custom		Document Number		Rev	
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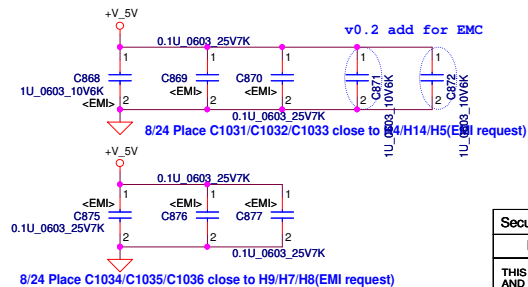
20K_0402 5% 10K_0402 5% 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100



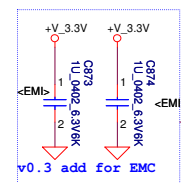
change net name from +5VALW to +5VSE



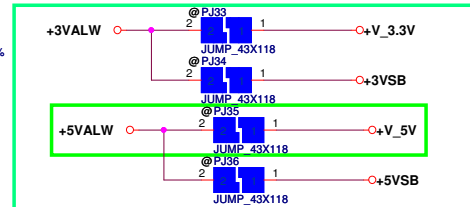
V0.3 add for EMC



8/24 Place C1034/C1035/C1036 close to H9/H7/H8(EMI request)



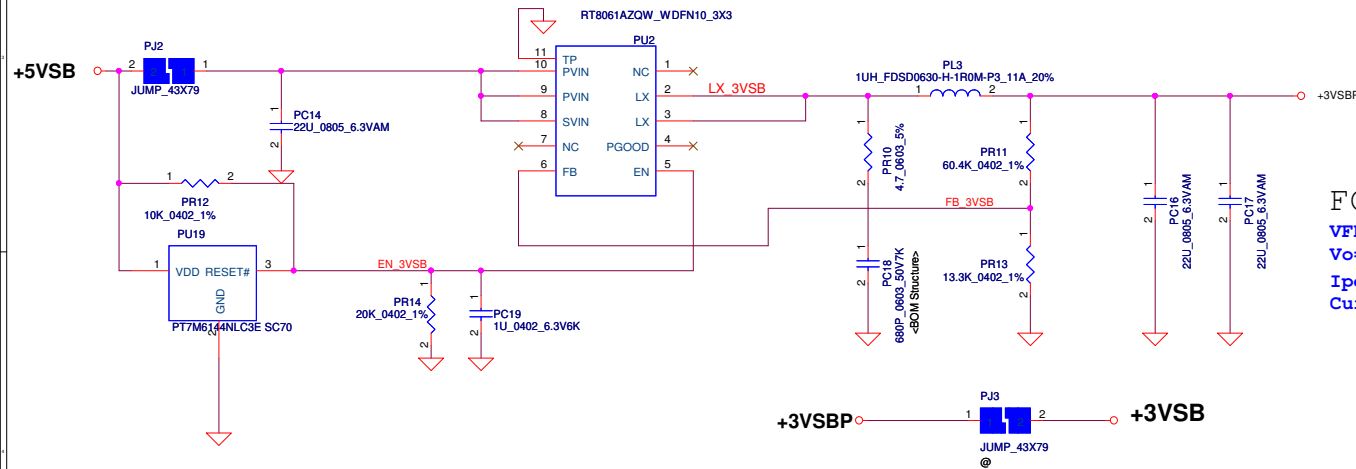
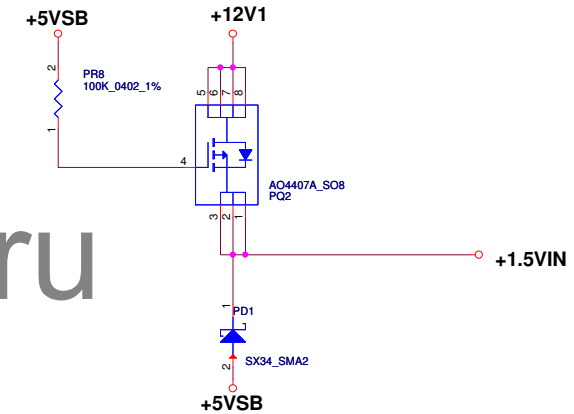
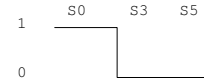
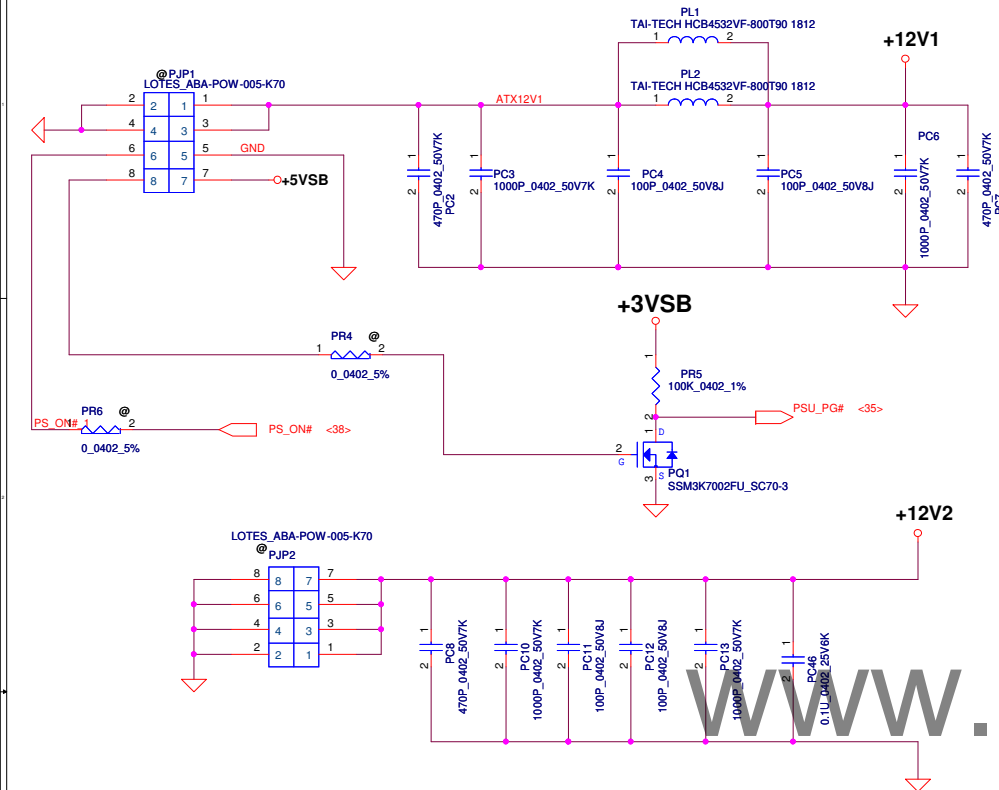
Abstract



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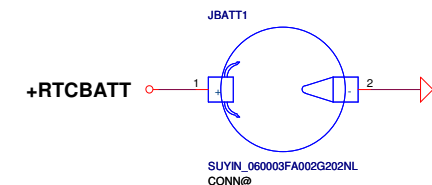
PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 57 degree C

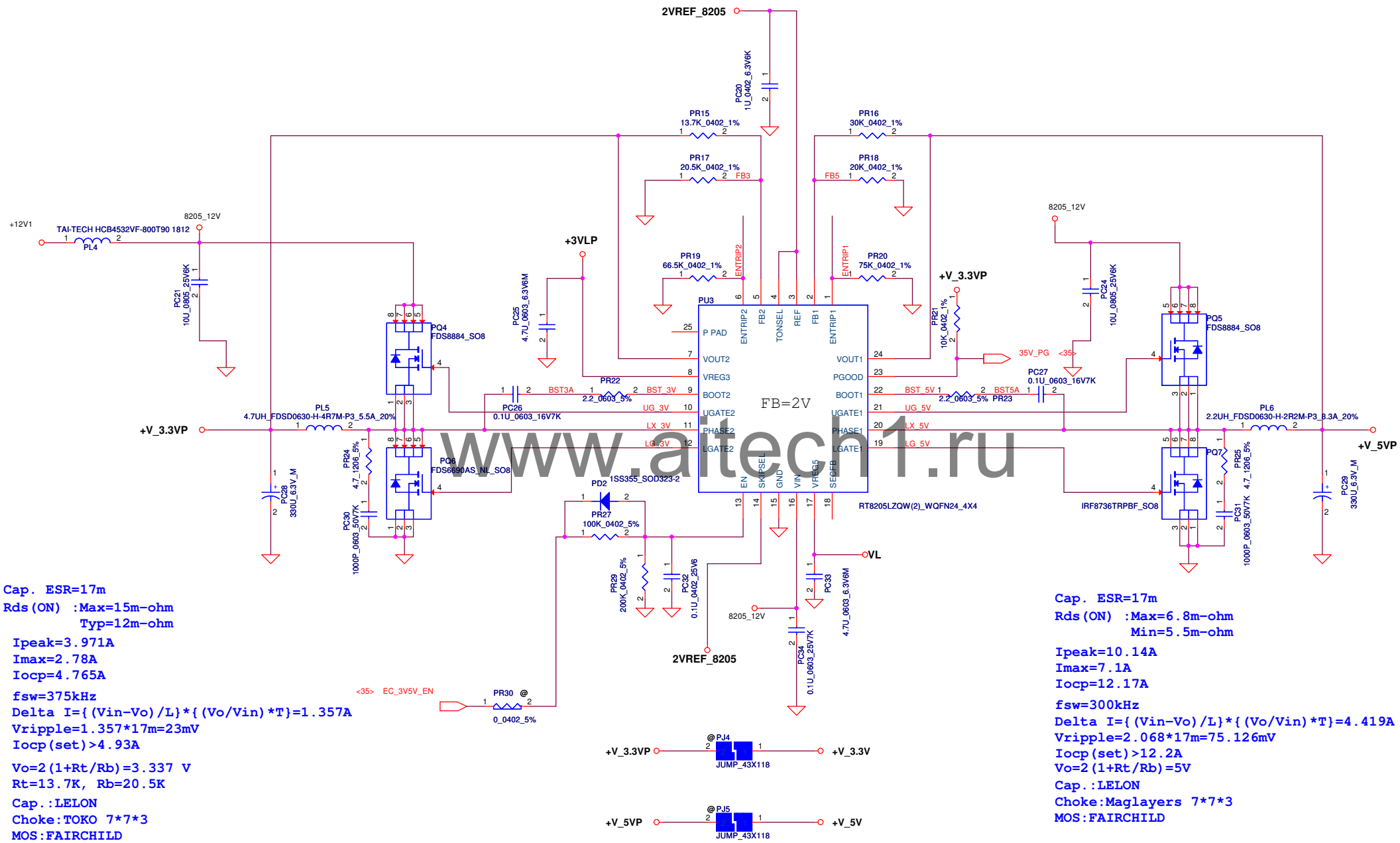


FOR EC suspend

VFB=0.6V
Vo=VFB*(1+PR7/PR9)=3.318 V
Ipeak=0.926A, Imax=0.7*0.755=0.648A
Current limit >4A



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Cap. ESR=17m
Rds (ON) :Max=15m-ohm
Typ=12m-ohm

Ipeak=3.971A
Imax=2.78A
Iocp=4.765A

fsw=375kHz
Delta I={ (Vin-Vo)/L }*{ (Vo/Vin)*T }=1.357A
Vripple=1.357*17m=23mV
Iocp(set)>4.93A

Vo=2(1+Rt/Rb)=3.337 V
Rt=13.7K, Rb=20.5K

Cap.:LELON
Choke:TOKO 7*7*3
MOS:FAIRCHILD
IC:RICHTER
Bead:
Diode: PANJIT

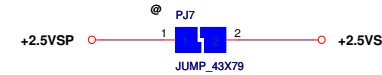
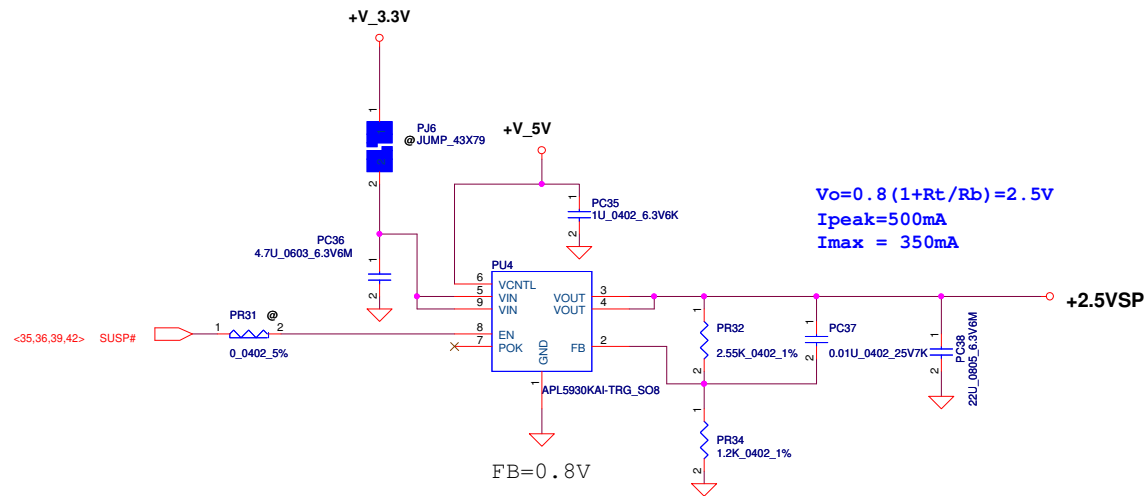
Cap. ESR=17m
Rds (ON) :Max=6.8m-ohm
Min=5.5m-ohm

Ipeak=10.14A
Imax=7.1A
Iocp=12.17A

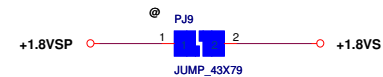
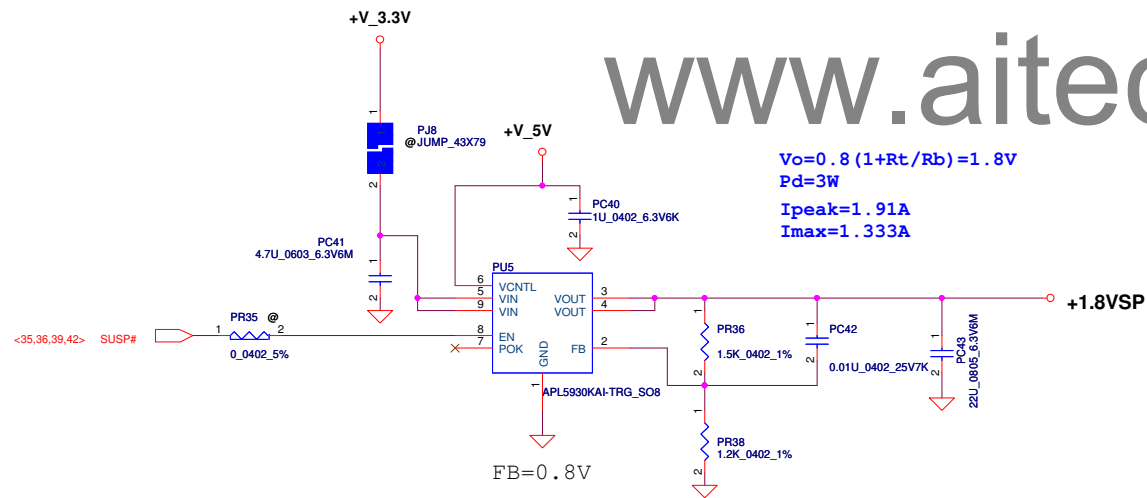
fsw=300kHz
Delta I={ (Vin-Vo)/L }*{ (Vo/Vin)*T }=4.419A
Vripple=2.068*17m=75.126mV
Iocp(set)>12.2A
Vo=2(1+Rt/Rb)=5V

Cap.:LELON
Choke:Maglayers 7*7*3
MOS:FAIRCHILD

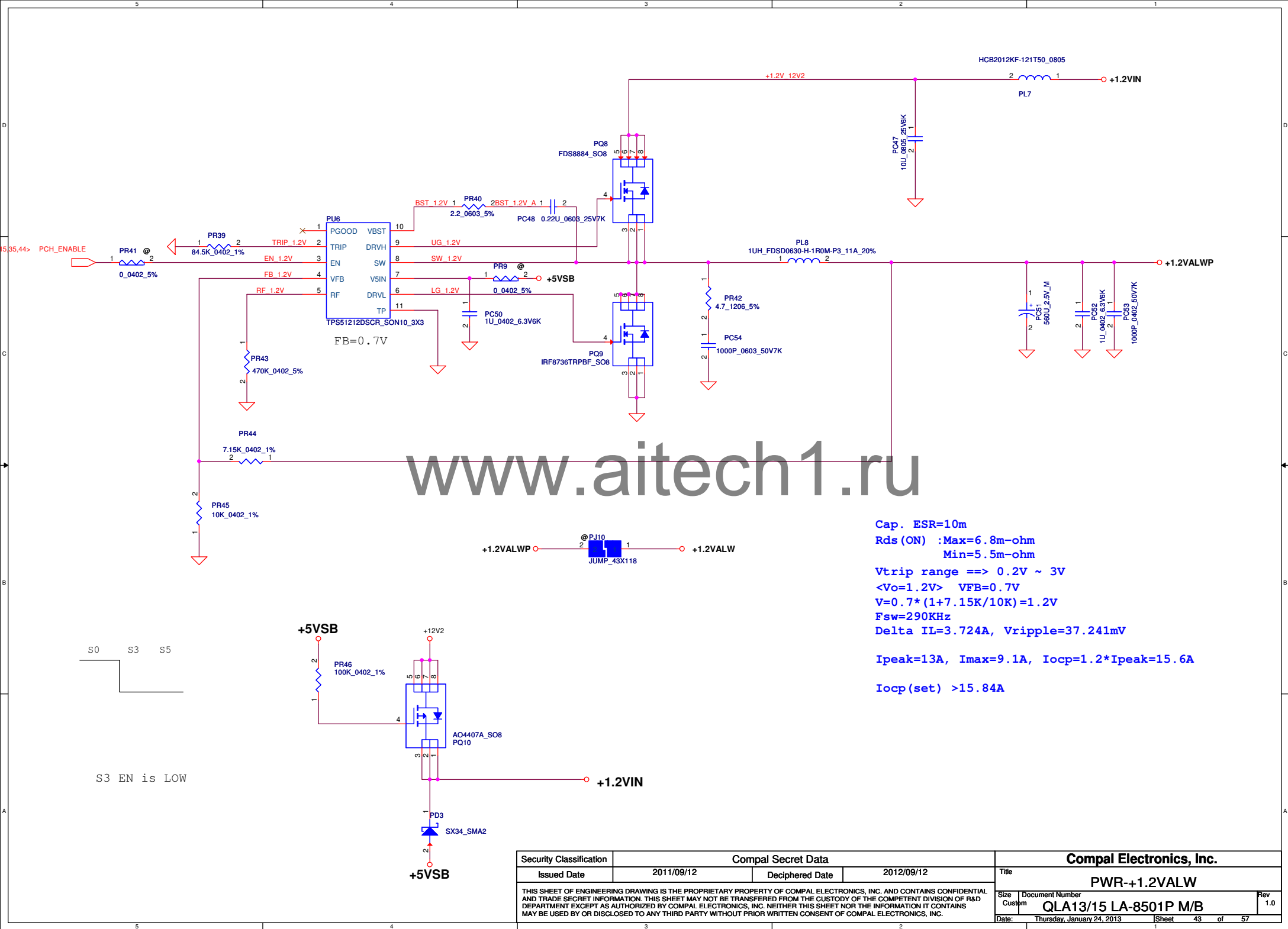
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Size	Document Number	Rev		Date	
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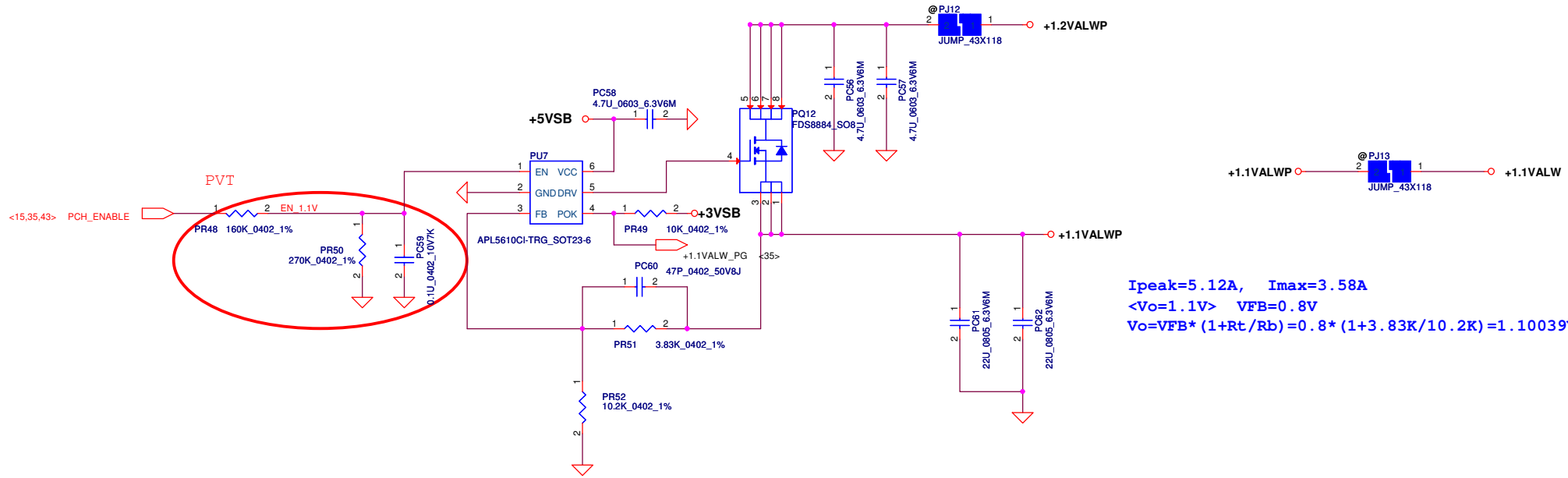
www.aitech1.ru



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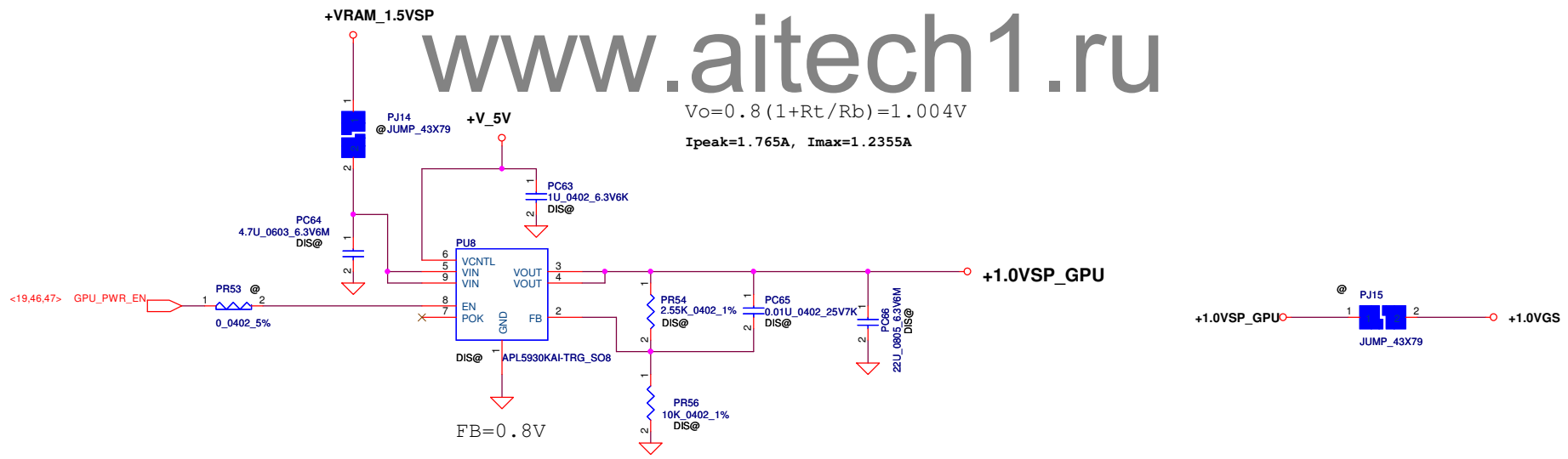
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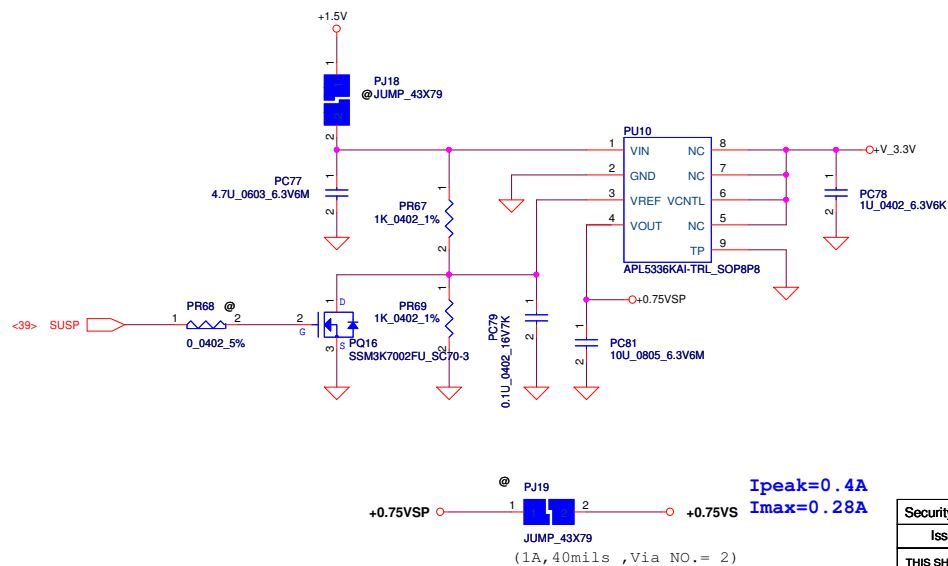
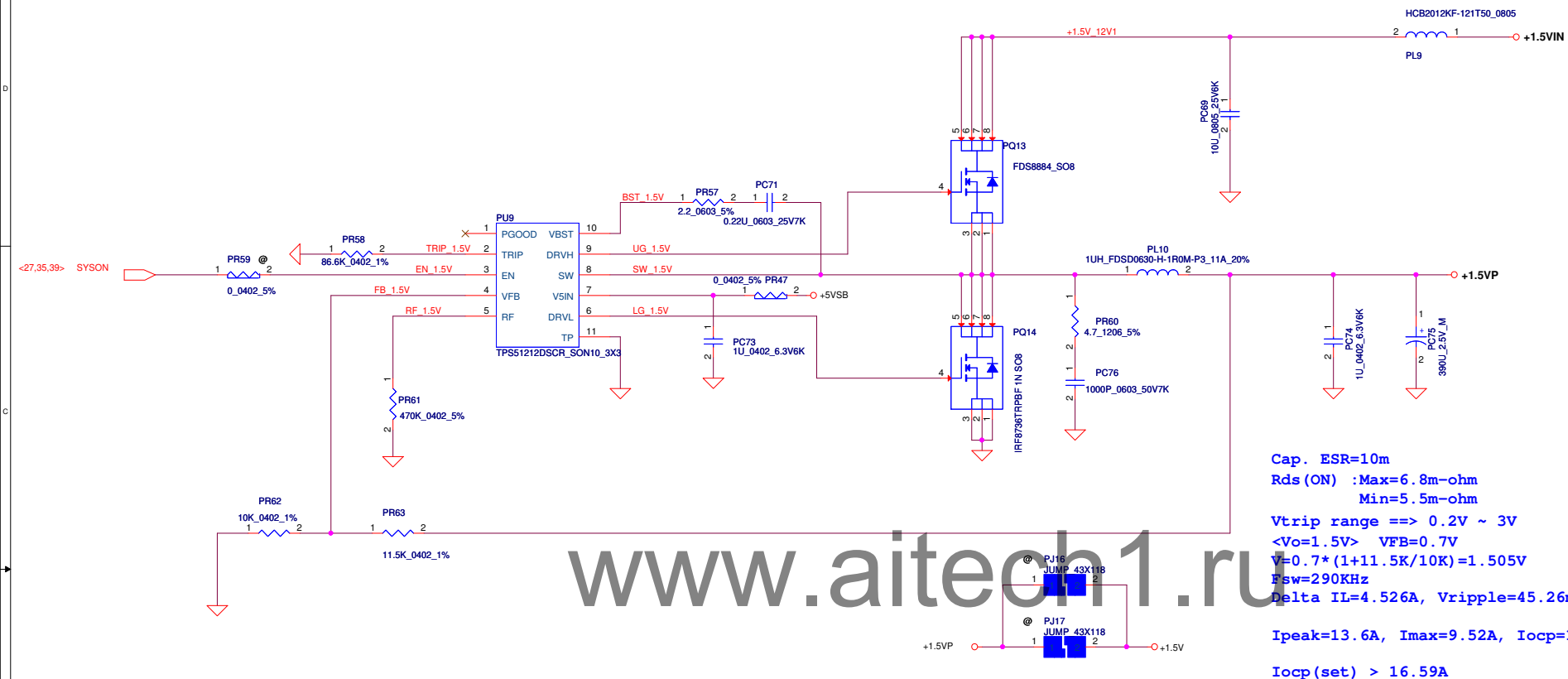
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 <Vo=1.1V> VFB=0.8V
 Vo=VFB*(1+Rt/Rb)=0.8*(1+3.83K/10.2K)=1.10039V

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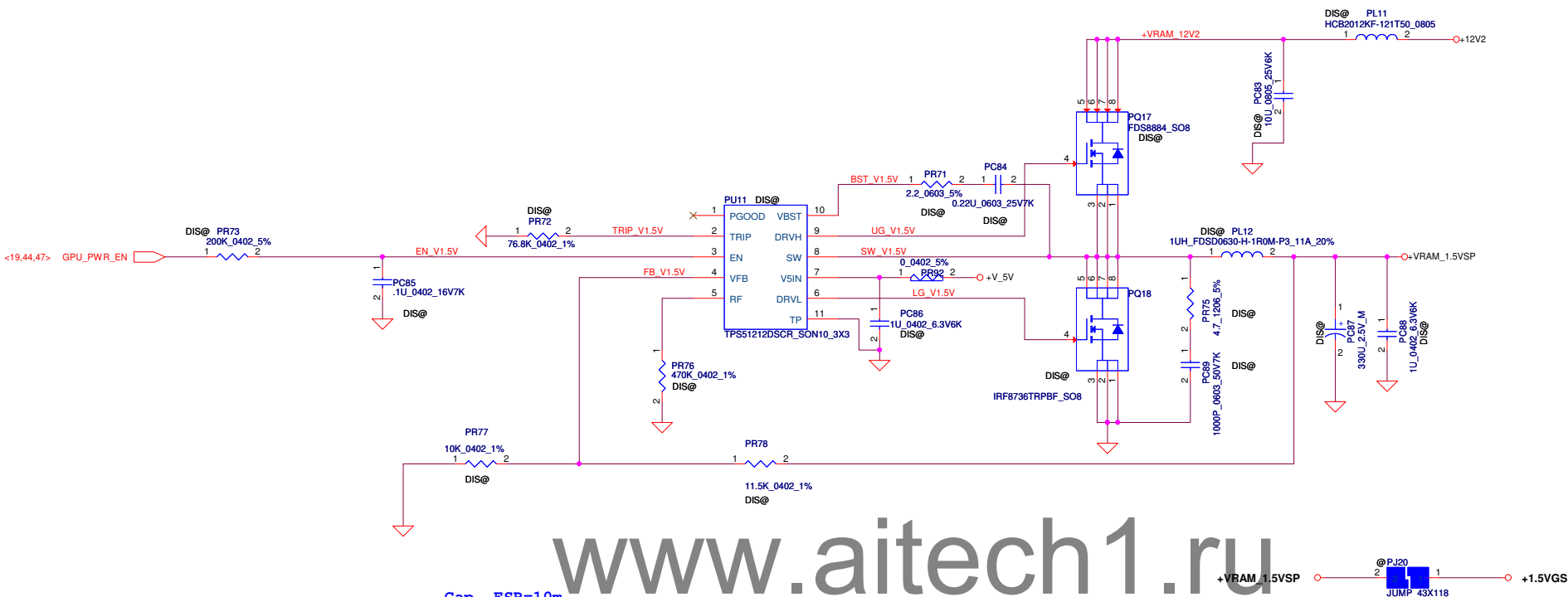
Vo=0.8(1+Rt/Rb)=1.004V
 Ipeak=1.765A, Imax=1.2355A



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								Date:	Thursday, January 24, 2013		Sheet 45 of 57

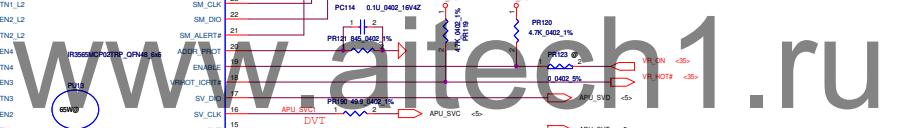


Cap. ESR=10m
 Rds (ON) :Max=6.8m-ohm
 Min=5.5m-ohm
 Vtrip range ==> 0.2V ~ 3V
 <Vo=1.5V> VFB=0.7V
 $V=0.7 * (1+11.5K/10K)=1.505V$
 Fsw=290KHz
 Delta IL=4.526A, Vripple=45.26mV

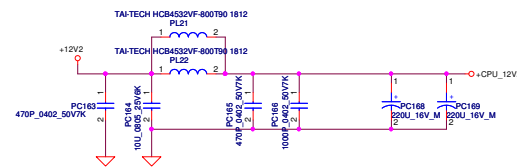
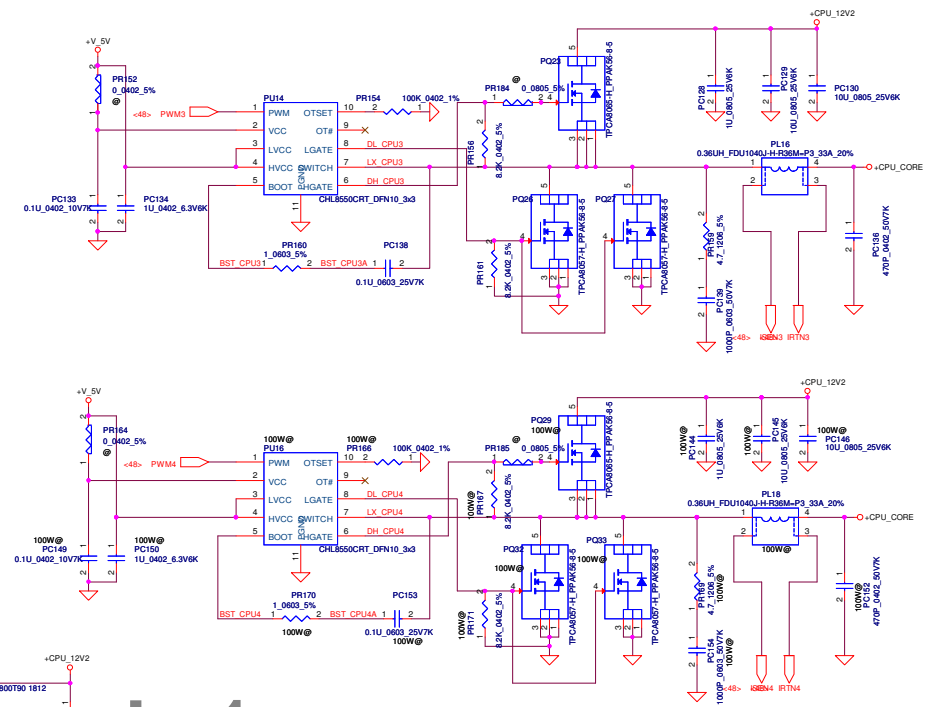
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Iocp(set) >14.97A

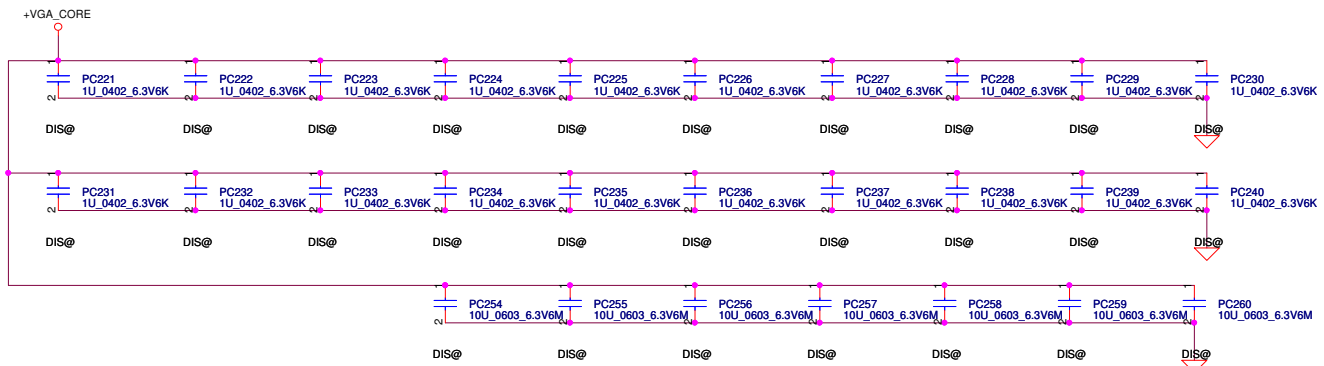
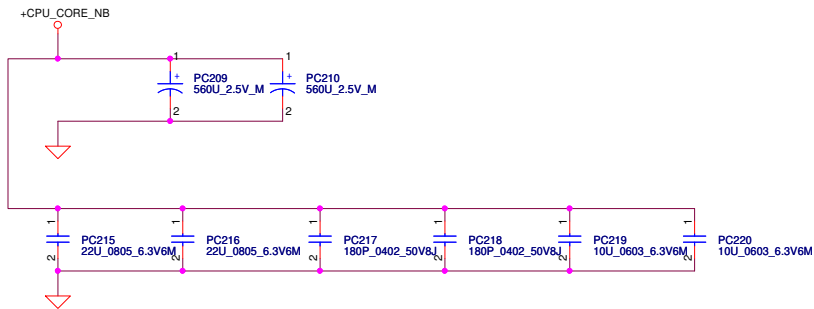
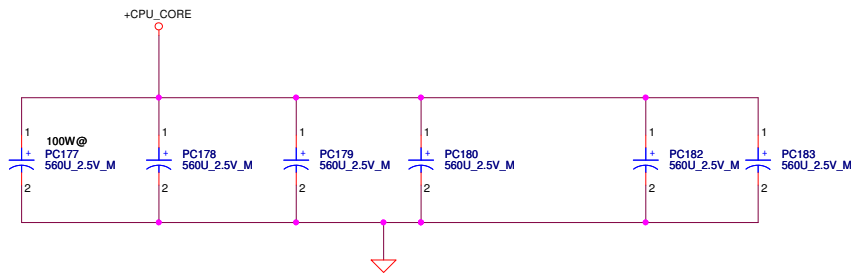
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Title PWR_CPU_CORE 1			
Size Custom	Document Number QLA13/15 1A-8501P M/B		Rev 1.



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				<p>QLA13/15 LA-8501P M/B</p>	
				Date: Thursday, January 24, 2013	Sheet 48 of 57

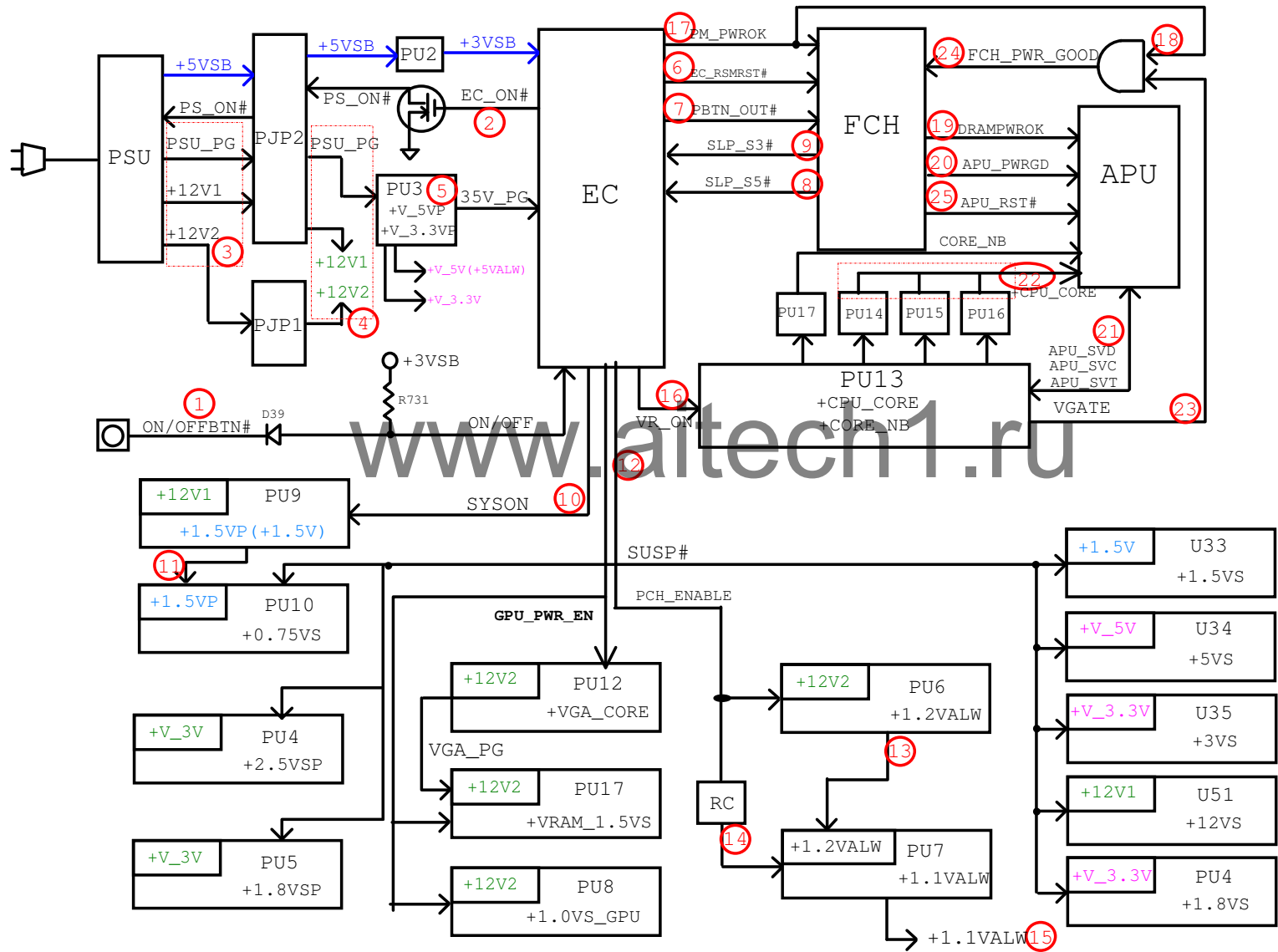


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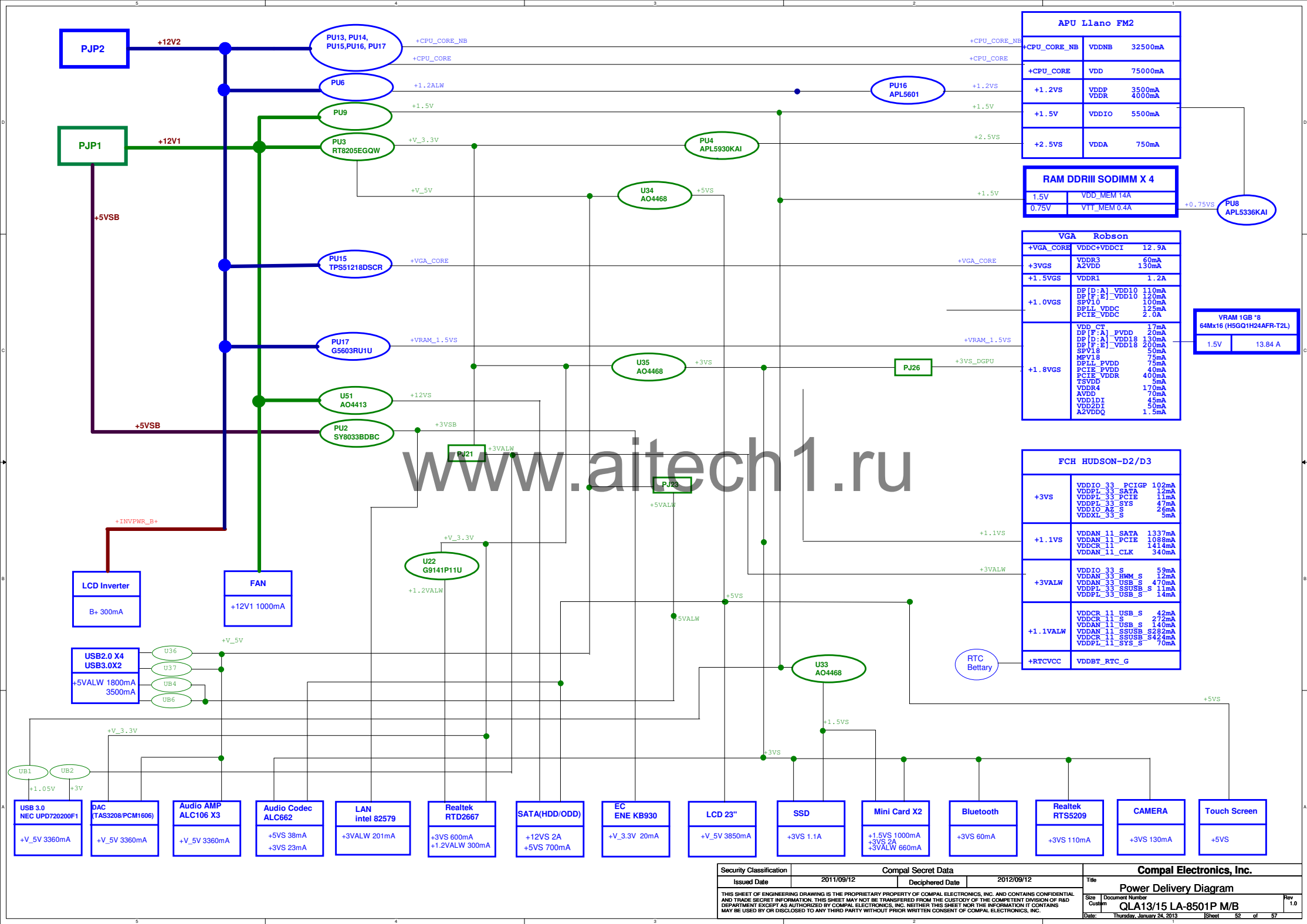
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Issued Date	2011/09/12	Deciphered Date	2012/09/12	Title	PWR_CPU_CORE 3
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MODEL NAME: QLA13 Power Sequence Block Diagram (Discrete)
PCB NAME: LA8501P
REVISION: 0.1
DATE: 2010/10/26

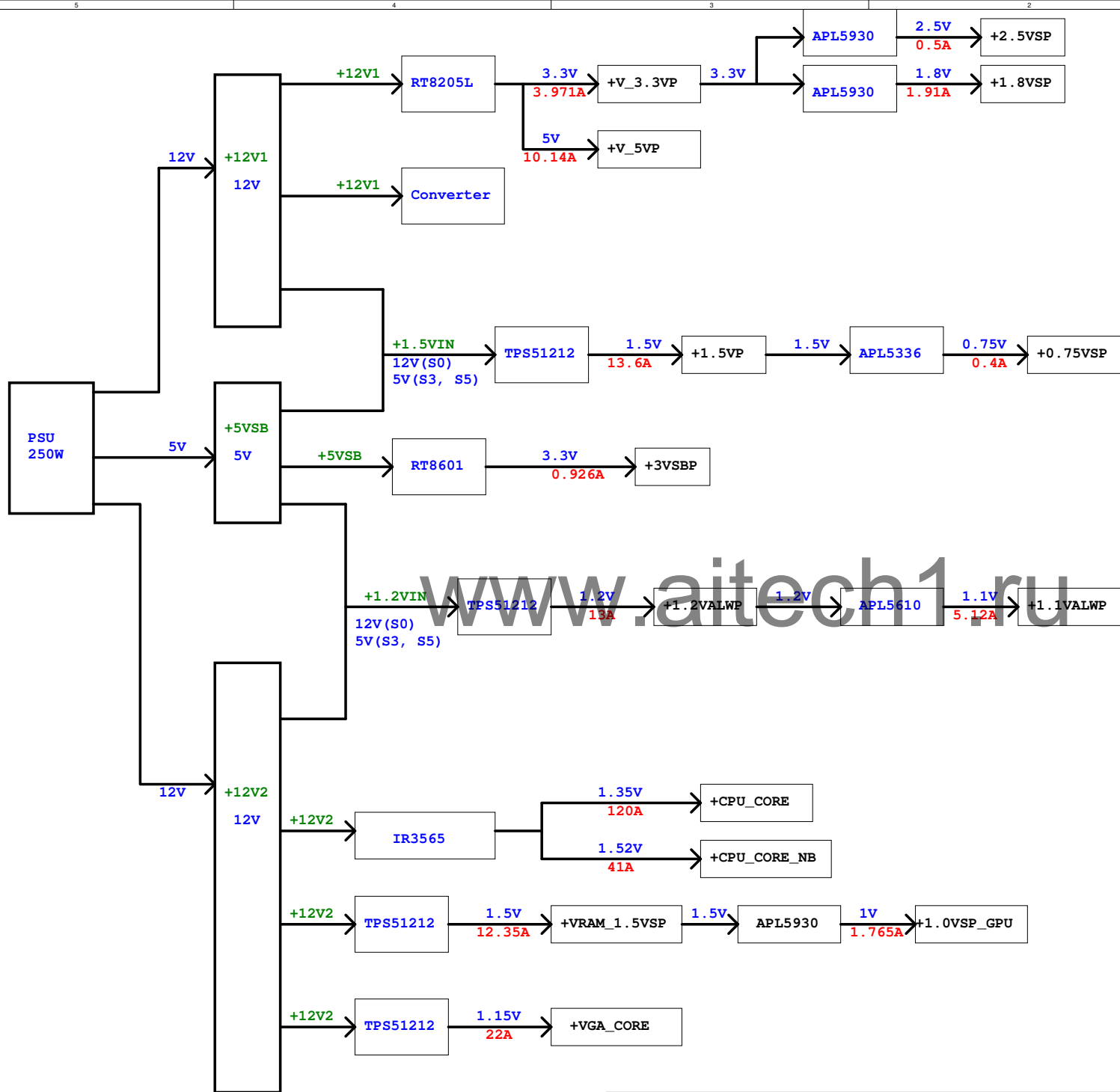


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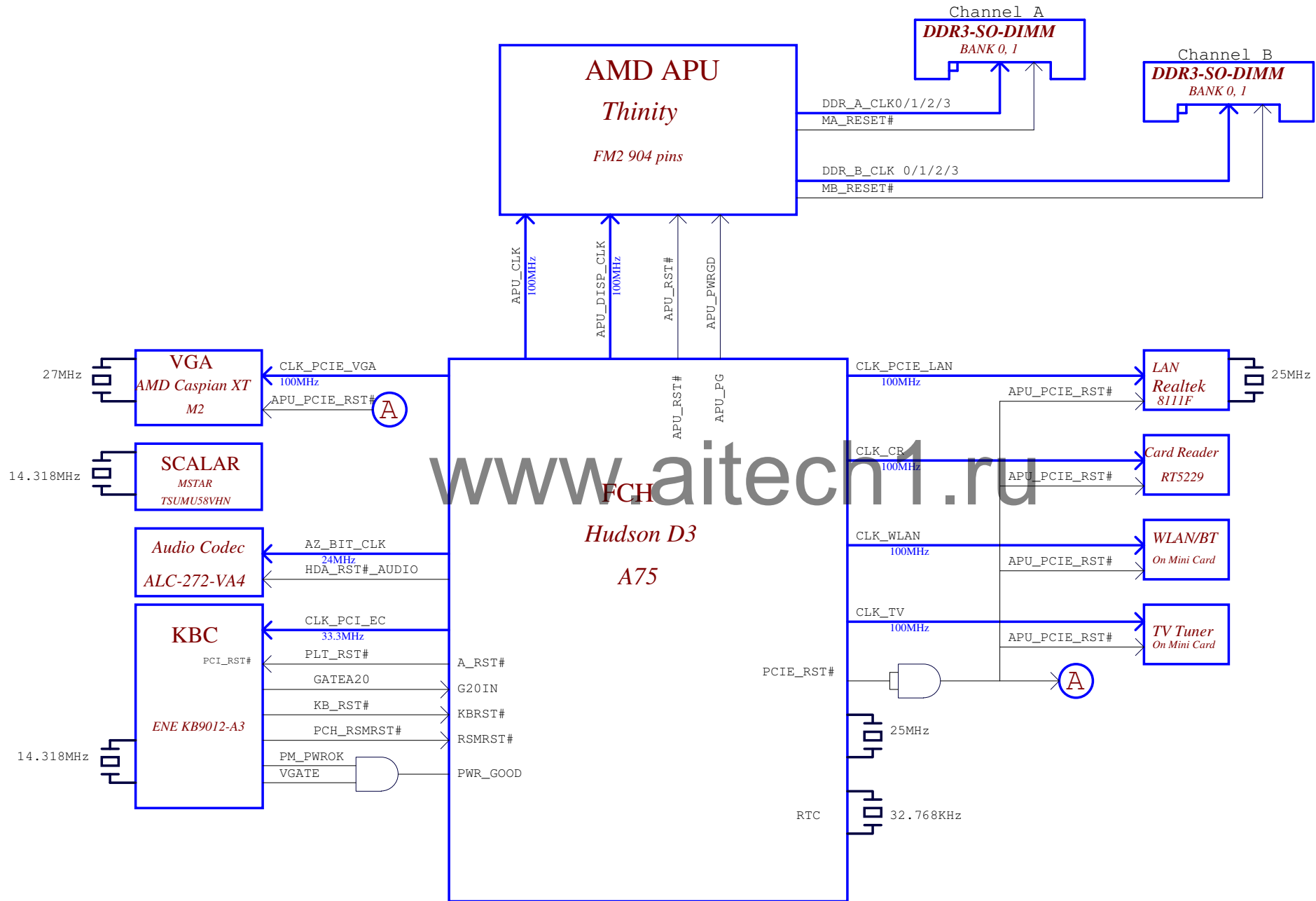
No	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2011/9/21	P50	Change PR88 to 10k ohm	Modify VGA_CORE VID setting value
2	2011/9/22	P47/P50	Change EN pin netname to GPU_PWR_EN	For RM request
3	2011/9/27	P50	Change PL14 connection to pin 1 and pin 4	For Layout
4	2011/9/28	P52	Change PC153 PIN2 to LX_CPU4	Modify PUI6 bootstrap circuit
	2011/9/28	P49/P49/P50	Change +1.2ALWP/+VRAM1.5VSP/+VGA_CORE input to +CPU_12V2	For layout easily
5	2011/9/28	P50/P52	Change PC90/P1/P2/P3/P26/P27/P29/P30/P42/P43/P45/P46/P56/P58/P64/P72/P73 PM from SE142106MD to SE00000QK00	For Cost saving
6	2011/9/28	P50/P46	Change PL13/PL7 PM to SM01000C000	For Cost saving
		P51	Net name+CPU_12V2	
		P50	Remove PC90	For Layout
7	2011/9/28	P43/P46	remove PR9/PQ3/PC9/PJ11/PK47/PJ11/PC55/PJ11	For Layout space
8	2011/9/29	P49	change PC87 From 390u/6h to 330u/4.2h	For Layout space
9	2011/10/03	P52	change PR146 PIN1 connect to PR148	IR FAE suggest
10	2011/10/03		change PC20,PC50,PC52,PC73,PC74,PC76,PC86,PC88,PC96,PC100,PC106,PC134,PC135,PC140,PC150,PC161,PC170to SE00000QK00	For Cost saving
			change PC25,PC31,PC36,PC41,PC56,PC58,PC64,PC77 to SE107475M80	
11	2011/10/04	P50	add PQ40	co-lay VGA
12	2011/10/04	P52	Modify PUI4 and PUI6 footprint form QFN10_3*3 to DFN10_3*3	Modify to correct footprint
13	2011/10/05	P50	Connect PL14 Pin2 to Pin1 & Pin3 to Pin4	For Layout shape
14	2011/10/11	P51	Modify PR97,98,149,150 connection	
15	2011/10/11	P51	Add short pad PR180	IR FAE suggest
			Change PR2,PR3,PR4 to SL300001000	For Cost saving
			Change PR146 to 500 ohm	OTP Tuner
16	2011/10/12	P49/P49/P50	Change +1.2ALWP/+VRAM1.5VSP/+VGA_CORE input to +12V2	For layout easily
		P51	Update PUI3 (TR3565) part number	New part number released
17	2011/10/12	P51	Update P146 to 499 ohm	old part a code
18	2011/10/14	P44/P46/P48/P49	Remove PC46/PC68 Change PC22/PC23/PC47/PC70/PC82 bom structure to *g* Change PC21/PC24/PC43/PC69/PC83 PM to SE00000QK00	For C38 request
19	2011/10/14	P43	add PC46/PC55/PC68	For ESD request
			add PR9/PR47/PR92/PR181	For C38 request
20	2011/10/14	P51	Change PC122 PM to SE026474K80	For PJE request
21	2011/10/17	P52	add PR182/PR183/PR184/PR185/PR186/PR187	For EMI request
22	2011/10/18	P52	change PR182/PR183/PR184/PR185/PR186/PR187 to 0805 size	For C38 request
23	2011/10/18	P52	Midify PUI4,15,PUI6,17 Enable Signal	Modify enable signal error
24	2011/10/25	P44	Remove PR26 in BOM	Modify PSU_PG signal
25	2011/11/09	P46	Change PR9 net name from +V_5V to +5VSB	
		P47	Change PC58 net name from +V_5V to +5VSB	Design change
		P51	Change PC58 net name from +V_3.3V to +3VSB add BOM Structure *g* at PR105 and PR106	
26	2011/11/14	P51	change PR105 and PR106 to 0805 size	
		P53	remove POSCAP PC184 and PC212 add BOM structure "100M" to PC177 add BOM structure *g* to PC181 and remove *g* from PC183 add PC244, PC245, PC246,PC247 add PC242, PC243, PC212, PC241,PC248,PC249 with BOM Structure*g* add BOM structure *g* to PC208	Design change
27	2011/11/16	P50	add BOM structure "D188" to PR88,PR90,PR93, PC221-PC260	BOM control
28	2011/11/17	P43, P48	change PM from SB0000009610 to SB0000009080 of PQ1,PQ15,PQ16	Material shortage
29	2011/11/18	P55	change PR93 to 27K, and PR88 to 20K	Design change
30	2011/11/18	P48	change PR47.2 net name from "+V_5V" to "+5VSB"	Design change
31	2011/11/23	P48	Add BOM Structure "100M" in PR116, PR117, PR118, PR122 and PC113	cost down
32	2011/11/24	P51	Add PR188 with BOM structure *65M*	
		P52	Add PR189 with BOM structure *g*	Design change
33	2011/11/28	P50	change PR88 to 10K and PR93 to 40.2K	
		P53	remove BOM Structure*g* of PC248	Design change
34	2011/11/29	P50	change PR107,PR112,PR116,PR124,PR128,PR133---1.58K change PR109,PR114,PR118,PR126,PR130,PR137---1.27K change PC109,PC110,PC133,PC115,PC117,PC131---0.47U(X78) PR144---2.05K PR135---1.78K PR145---1.82K	Design change
		P46,P49	change PR57, PR71 to 282	
35	2011/12/01	P51	add PR191-4.7K add PR190-49.5-ohm add PDS add PR188	
36	2011/12/7	P50	Change PR86,PR88,PR90,PR93 resistor value	Change VGA_CORE VID
		P43	remove BOM Structure*g* of PC46	For EMC request
37	2011/12/13	P51	Add PUI3 BOM Structure *63M* for SA00005I200 Add PUI3 BOM Structure*100M* for SA00005B90	Part Number divided
38	2012/1/31	P43	PUI2 change to SA00003R000 (SY8033)	Design change
		P50	PR139,PR145 change to 1.96K	Loadline finetune
		P47	PC59=0.10F , PR48=160K , PR50=270K	Design change
39	2012/2/1	P43	PUI2 change to SA00004CY10 (XT8061) Add PUI9	Design change Design change
40	2012/10/29		Change 0 ohm res to short pad	low cost
41	2012/11/09		Remove component with BOM Structure *g*	For layout
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Clock and Reset Diagram



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HW schematic change list

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	01/20	P15	R1764 change to 1M	BOM ERROR
2	01/20	P18	R1737,R1738 BOM change to @	BOM ERROR
3	01/20	P29	Add R1803	For HDMI Votage
4	01/20	P40	C612 change to 0805	For DFX
5	01/20	P40	JBT1 change to 8 pin ACES_87212-08G0L	For ASSY to move location
6	01/20	P31	Remove R525,C681 & R524,C681	For EMI
7	01/28	P42	H2,H4 change to 4P0	For ME
8	01/28	P42	Add 10u C1908,C1909 for +V_5V	For ESD
9	01/28	P39	Add 1u C1906,C1907 for +V_3.3V&+USB_VCCA	For ESD
10	01/28	P29	Add C1910,C1911 for +V_3.3V	For HDMI IN Re-driver
11	01/28	P29	Remove ESD DIODE D12,D13,D16,D18	For HDMI IN Re-driver
12	01/29	P05	Remove HDT1	For ESD
13	01/29	P31	Remove Q102,Q120	For EMI
14	02/01	P41 P39 P29 P37 P40 P16	Add C1916 0.1u on SENSE_FB_3V5B Add C1914 0.1u on S3USB_ON Add C1912 0.1u on IO Conn_13VALW Add C1913 0.1u on MUTE_CODEC Add C1915 0.1u on BT_RESET Change C247 2.2u to 10u	For ESD
16	02/24	P33 P39 P40	Add RC on external& internal USB D-	AMD Errata 40
17	03/16	P37	Add PWR_65W#100W GPIO	
18	03/19	P28	Add PANEL_C_2	
19	04/16	P41	Del SW1	
20	05/04	P29	Add D10/D11 for ESD	
21				
22				
23				

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				<div> <div>Sheet</div> <div>56</div> </div> <div> <div>of</div> <div>57</div> </div>	

HW schematic change list

1	P5	APU	Remove HDMI , DP ,DDC , AUX, HPD signal	
2	P18	VGA	Add HDMI,DDC HPD signal add R1203~R1205 R1260 Pop R1737 R1738	
3	P24	HDMI SW	Remove the HDMI to HWTv trace Remove R368-R375 for switch HDMI Remove for HWTv terminator	
4	PXX	RTS2136	RTD2136S Full Page Delete	
5	PXX	HWTv Conn	HWTv Conn Full page delete	
7	P26	Scaler	Scaler remove SW2 and peripheral	
8	P27	IO Conn	Remove the HDMI_IN signal Change the HDMI Netname Remove the CVBS Signal	
9	P33	HP Conn	Remove Analog SW (U28), TV HP Driver (U32) Connect the HP to Jack directly	
10	P34	AMP	Remove Analog SW(U104) , U36,U34 Connect the AMP to SPK directly Remove R610 and TV_AMP_MUTE	
11	P35	EC	Remove for HWTv RTD2136	TUNER_PWR_ON AV_AUDIO_SEL# EC_HWTv_PWRON SOURCE# HPCOUT_SEL AMPIN_SEL LVDS_ON# TV_ON_OFF HW_TVID1 HP_AMP_DOWN# TV_AMP_MUTE

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